TM 11-6125-258-34

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL

STATIC POWER INVERTER PP-7274B/A
(EMP MODEL 3-PS-277-3)
(NSN 6125-00-148-8342)

HEADQUARTERS, DEPARTMENT OF THE ARMY

10 DECEMBER 1980

WARNING

PRECAUTIONARY DATA

Personnel performing instructions involving operating procedures and practices which are included or implied in this technical manual shall observe the following precautions. Disregard of these warnings and precautionary information may result in injury, death, or an aborted mission.

HANDLING CLEANING AGENTS

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internal ly, consult a physician immediately.

USE OF COMPRESSED AIR TO DRY PARTS

To be usable for cleaning, the compressed air source must limit the nozzle pressure to no more than 30 pounds per square inch gage (PSIG). Goggles must be worn at all times while cleaning with compressed air.

HAZARDOUS VOLTAGES AND HIGH CURRENT

To avoid electrical shock, be extremely careful when making required measurements and adjustments.

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WASHINGTON, DC, *10 December 1980*

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REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.

In either case, a reply will be furnished direct to you.

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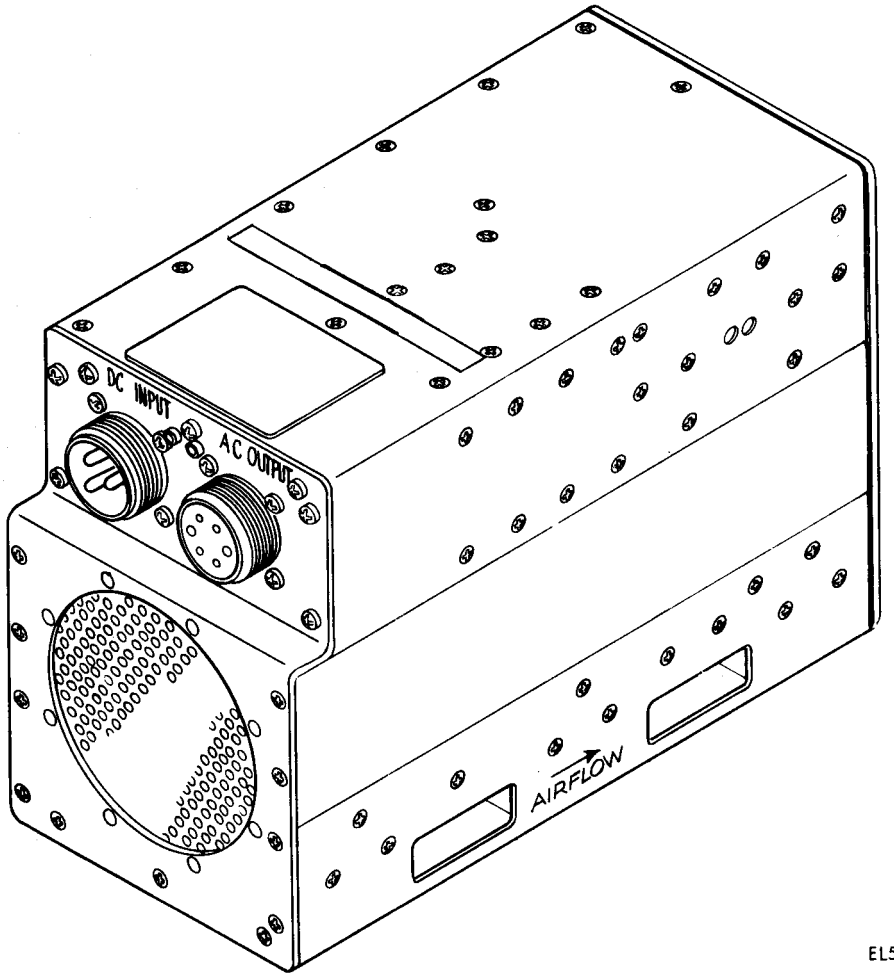


Figure 1-1. Inverter.

CHAPTER 1

INTRODUCTION

SECTION 1. GENERAL

1-1. Scope

This manual contains the general and direct support maintenance instructions for the Static Power Inverter PP-7274B/A (EMP Model 3-PS-277-3) (inverter).

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

1-3. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System.

b. Report of Packaging and Handling Deficiencies. Fill out and forward Standard Form 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/ NAVSUPINST 4440.127E/AFR 400-54/MCO 4430.3E and DSAR 4140.55.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your Static Power Inverter PP-7274B/A needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Tell us why a procedure is hard to perform. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703. Well send you a reply.

1-5. Administrative Storage

a. If inverter is to be stored for longer than 3 years, operate inverter for 1 hour before storage. After 3 years in storage, remove inverter from barrier material and operate inverter for 1 hour. Inverter may be returned to storage for another 3 years. Inverter can be stored for a maximum of 10 years. After this time, the electrolytic capacitors in the input capacitor bank must be replaced.

b. Install plastic caps on connectors J1 and J2. Position inverter in barrier material (Specification MIL-B-131). Install two units of desiccant dehydrator (Specification MIL-D-3464) into barrier material and heat seal barrier material.

c. It is desirable that storage temperature not exceed 37°C but shall not exceed 53°C. For further information on storage requirements, refer to TM 740-90-1, Administrative Storage.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Purpose and Use

Static Power Inverter PP-7274B/A (EMP Model 3-PS-277-3) converts a nominal 28 vdc input to a 400 Hz, 3 phase 115 vac output, and is generally intended for use in aircraft.

1-8. Description

The inverter (fig. 1-1) converts +28 vdc into 115.5 vac rms, 400 Hz, 3 phase at 750 va. The input (J1) accepts the +28 vdc (input current up to 41 amp) where it is sent to the input filter. The input filter removes

any voltage spikes and rf noise that may be present on the input power cable. The input voltage is then sent to the input capacitor bank and voltage regulator. The input capacitor bank stores the + vdc in case instantaneous output power requirements demand more than the input power supply can produce. The voltage regulator regulates the fluctuating +28 vdc into +16 vdc to supply power and control voltages to the rest of the internal circuitry. A sample of the 115 vac is fed back to the oscillator regulator to adjust the transformer input to compensate for any change in power demand for the inverter. The inverter will automatically limit output current if the output power exceeds 2.5 times its rated load and will remain limited until the overload condition is removed.

1-9. Tabulated Data

Table 1-1 and table 1-2 show the electrical and physical specifications of the inverter.

Table 1-1. *Electrical Characteristics*

Parameters and conditions	Values
Input voltage	+28 vdc
Input current	41 amp maximum
Output voltage	115 ± 2.5 true rms
Output power	250 va at 2.18 amp per phase
Output frequency	400 ± 7 Hz
Output distortion	5% thd maximum
Efficiency	65% minimum
Load power factor	0.95 capacitive to – 0.78 inductive
Overload	50 vac minimum at 200% rated current for 5 seconds.
Short circuit	Internal protection is provided at 250% rated current for 5 seconds minimum into a short circuit, automatic current limiting will then occur after 5 seconds limiting short circuit current to 150% (approximate rated current). Unit will recover automatically (into any rated load) within 0.5 second upon removal of short circuit (or overload).
Reduced input voltage	Unit will provide 110–117.5 vac (at any rated load) with input between 18 and 26 vdc. Unit will not be damaged with input between 0 and 18 vdc.
Excessive input voltage	May be operated for 5 minutes maximum. Between 29 and 32 vdc unit will meet all transient and surge requirements.

Table 1-2. Physical Characteristics

Parameters and conditions	Specifications
Overall dimensions	Height: 8.00 inches maximum Width: 5.50 inches maximum Length: 11.50 inches maximum
Weight	23 pounds maximum
Operating temperature range	–55°C to 85°C (–67°F to 185°F)
Cooling	Internal fan

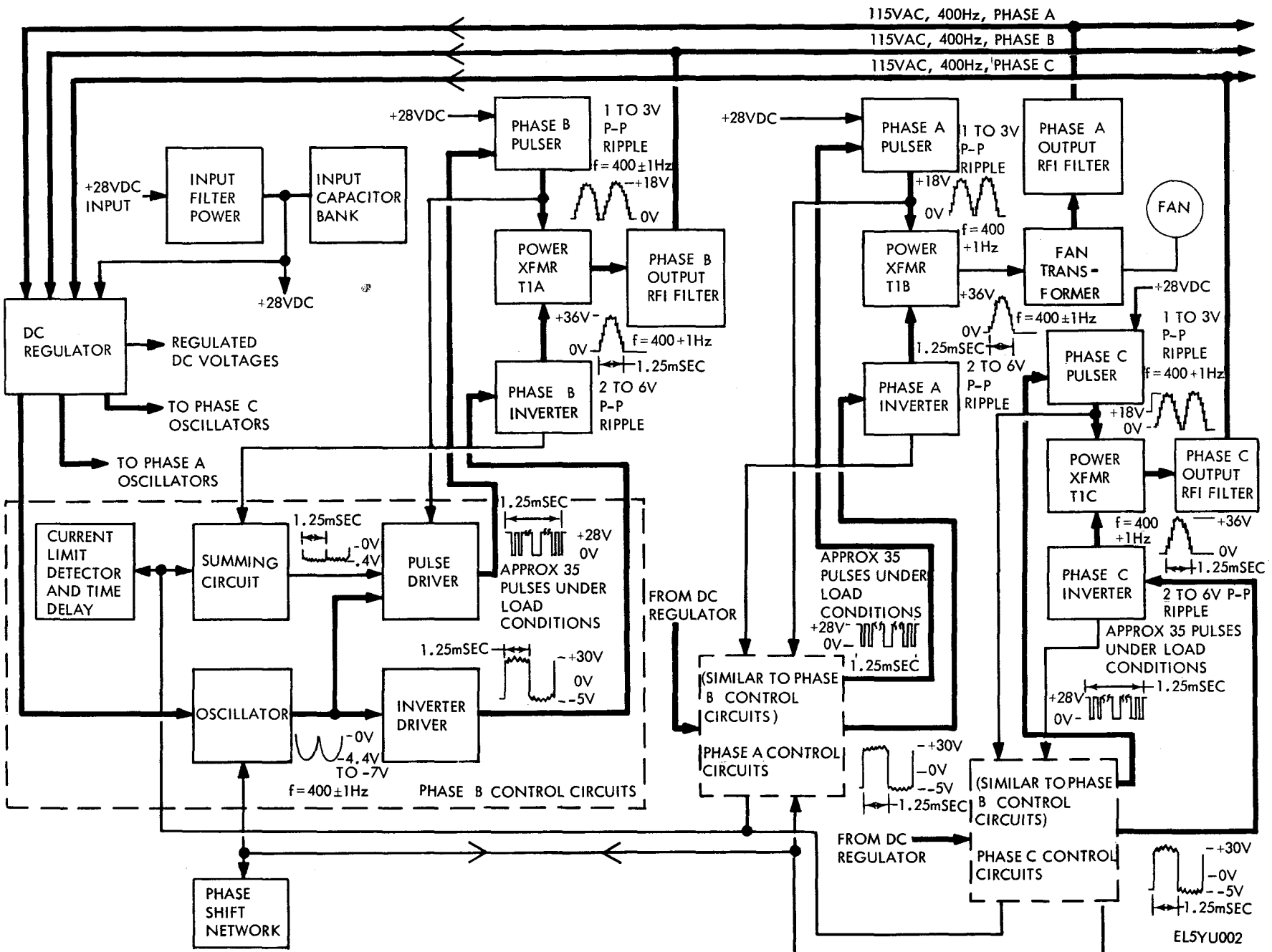


Figure 2-1. Block Diagram Simplified.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section 1. BASIC FUNCTIONAL OPERATION

2-1. Unit Functional Description

(fig. 2-1 and FO-1)

a. The inverter converts a +28 vdc input to a regulated 115 vac 400 Hz, three phase output through the use of pulse modulation.

b. The *+28* vdc input is filtered by the input filter to eliminate any rf signals which may be present on the input cabling and to prevent random spikes and rf energy generated by the pulser circuits from being transmitted back to the external +28 volt line. The input capacitor bank stores energy to meet the very large but irregular current demands made by the pulser circuit.

c. The +28 vdc input is also applied to the dc regulator, which provides regulated dc voltages to the control circuits and oscillator circuits. A sample of the 115 vac output is compared with a zener reference voltage in the regulator to provide control voltage to the oscillator, the output amplitude of which varies inversely with changes in the 115 vac output.

d. A negative, half wave rectified output from the oscillator is applied to the inverter driver, and a negative, full wave rectified output is applied to the pulse driver. The inverter driver squares the input signal and provides a push-pull square wave output to the inverter circuit.

e. The pulse driver receives three inputs; the full wave rectified; 400 Hz oscillator signal; a pulser feedback signal; and an overcurrent signal. The pulse driver output is a series of pulse groups of fixed amplitude whose duty cycle varies with output voltage and current.

f. The 400 Hz oscillator signal provides the basic timing and control voltage for the puke driver. Since a sample of the 115 vac output is fed back through an output adjust potentiometer in the dc regulator circuit to the oscillator, any variations in the output voltage or any adjustments in the voltage setting will be reflected in the oscillator signal level. The pulser feedback signal, which varies with the output load current sensed in the pulser integrator circuit, is compared with the oscillator signal and the resulting voltage controls the duty cycle of the pulse driver output. As the output load current increases for a given output voltage level, the pulse driver will sense a larger pulser duty cycle. The increased duty cycle of the pulse driver's output will cause the pulser to gate more current from the +28 vdc supply to the pulser's integrator circuit. This action will meet the increased current demands in the load circuit while maintaining the desired voltages; conversely, a decreased load current demand will cause the pulse driver to decrease the duty cycle applied to the pulser circuit. The pulser will gate less current from the +28 vdc supply, and the lower current requirements of the load will be met without an increase in the output voltage.

g. A sample of the output load current flowing in the inverter circuit is applied through the summing circuit to the current limit detector and time delay circuit. Should the output load current exceed 1.5 times the rated load current, the circuit will provide an overload signal through the summing circuits to the pulse driver. As a result, the duty cycle of the pulse driver will decrease to a value which controls the output load current at 1.5 times the rated load current. The inverter continuously maintains an overload of 1.5 times the rated load.

h. Should the overload exceed 2.5 times the rated load current, the feedback signal from the inverter circuit will swamp the biasing voltage in the summing circuit and an immediate overload signal will be applied to the pulse driver. Since no buffering circuits are involved at this time, the overload signal will cycle on and off as the output load current is alternately cycled to 1.5 times rated load and to its former overload value. This cycling will continue for approximately 5 seconds, after which the current limit detector and time delay circuit will energize and reduce the output load current to 1.5 times rated load.

i. The outputs of the pulse driver and inverter driver are applied to the pulser and inverter circuits respectively. The output of the pulser is applied to the center tap of power transformer T1 and the outputs of the inverter circuit gate on alternate halves of T1's primary winding to obtain a complete sine wave on the secondary.

j. The pulser consists of a series of current switches which are pulsed on and off as required gating current from +28 vdc supply to the integrator network. The output of the integrator circuit is a full wave rectified

sine wave which is gated in the primary winding of T1 to provide a sine wave output in the secondary winding of T1. It should be noted that the integrator network includes the LC network in the pulser, transformer T1 and a shunt capacitor in the output circuit (fig. FO-2).

k. The output of T1 is applied through the output RFI filter, where random spikes and rf energy generated by the switching circuits are removed. Also, a sample of the 115 vac output is applied to the ac output adjust circuit in the dc regulator.

2-2. Repetitive Circuits

a. Detailed explanation of the individual circuits has been limited to the phase A circuit only. Table 3-2 gives a cross-reference of reference designations for phases B and C. Notice that the current limit and dc regulator circuits are not duplicated for phases B and C. These two circuits are designed so that the oscillator, pulser driver, inverter driver, pulser and inverter are connected in parallel. This was done for ease of regulation of the control voltages of all three phases. Refer to paragraph 2-7 for explanation of the dc regulator.

b. The current limit circuit, located on PCB B16, is also designed so that the summing circuits are connected in parallel. Refer to paragraph 2-13 for a detailed explanation of the current limit circuit.

2-3. Output Phase Configurations

The inverter is a 400 Hz, 3 phase system. This inverter has the capability of operating in three different output modes. By externally connecting the pins of J2 as shown in figure 2-2, the inverter can operate in either the Delta or WYE mode.

2-4. Internal Phasing

a. The internal phasing of the inverter is done by the phase lock circuitry of the phase A oscillator. The combination of L1 and L101 on the B25 board and the secondary of L101 on the B26 board develop the phase pattern for the inverter.

b. On the output of a 3 phase system, phase A is the primary phase and phases B and C are dependent. In referencing phases B and C to phase A, phase B will lag phase A by 120 degrees, and phase C will lag phase A by 240 degrees. A 400 Hz signal has a repetition rate of 2.5 milliseconds. Assuming that the phase A signal is at zero volts, phase B will be 0 volt 0.83 millisecond later and phase C will be 0 volt 1.66 milliseconds after phase A.

NOTE

The figures 0.83 ms and 1.66 ms are only valid when the basic frequency is 400 Hz.

c. Refer to figure 3-4 for phase relations between phases A, B, and C at the oscillator.

d. The following paragraphs (para 2-5 through 2-14) give a detailed description of the circuits in the inverter. Reference designations used in the descriptions are of the phase A circuits. Table 3-2 will cross-reference the designations to phases B and C.

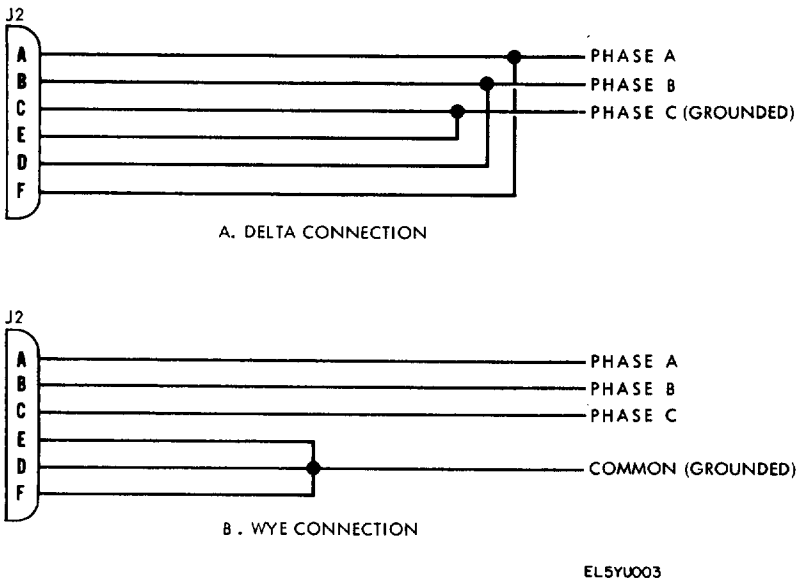


Figure 2-2. Output Connection Diagram.

Section II. FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

2-5. Input/Output EMI/RFl Filter

a. +28 vdc is applied through pins A and C of J1 to the low pass input filter (fig. FO-2). The input voltage can vary from +26 vdc to +29 vdc and is capable of supplying load currents up to 41 amperes. Capacitor C501 and C502 shunt high frequency noise that is generated either externally or internally to ground. Inductor L501 is a high frequency choke which presents a high impedance to voltage spikes or rf impulse noise that may be present on the +28 vdc bus.

b. The output filter is used to remove high frequency noise, which is generated by the pulser and inverter circuits, from 115 vac, 400 ±7 Hz output.

2-6. Input Capacitor Bank

The input capacitor bank (fig. FO-2) acts as a storage cell for the inverter. Nominal +28 vdc is applied from the input falter through the +28 vdc bus to capacitors Cl through C17. The capacitor bank provides an additional source of current to supply the pulser circuits when instantaneous demands by the pulser exceed the capacity of the +28 vdc source. The bank, by virtue of its faltering action, also aids the input filter in eliminating voltage spikes and rf noise generated by the pulser.

2-7. Dc Regulator

a. The dc regulator (fig. FO-3) provides regulated voltage to the control and oscillator circuits. The regulator is located on printed circuit boards B26 and B28. Potentiometer R109 adjusts the regulated dc voltage to the oscillator circuits.

b. The dc regulator consists of a series regulator, ac error detector and an oscillator regulator, all of which are located on B26. The Darlington pair Q101 and Q102 form the series regulator. This provides the necessary high gain and low output impedance necessary for regulation.

c. Zener diodes CR102 and CR103 provide a +18 vdc referene level for the regulator. The + 16.6 vdc output of the series regulator is applied through current limiting resistor R138 to the base of Q16, which is located on printed circuit board B28. A second output from the regulator provides + 16.5 vdc to the control circuits.

d. A 24 volt RMS sample of the 115 vac output is obtained from voltage divider R31-R29 located on the voltage regulator module B28 and is applied to the anode of CR114 and CR101. CR114 and CR101 rectify the ac voltage into pulsating dc. The pulsating dc is filtered and stepped down further, and is compared with a +6.8 vdc zener reference voltage by ac error detector Q103. The output of Q103 controls the dc level that oscillator regulator Q104 applies to oscillator Q105.

2-8. Oscillator

a. The oscillator (fig. FO-3) is a shunt fed Hartley type. Tuning is accomplished by selecting C104 to achieve 400 ±0.5 Hz at the oscillator output.

b. The 400 Hz oscillator provides the basic timing control voltage to the inverter. Oscillator input is a negative going, full wave rectified signal which varies from -4.4 to -7.0 volts peak depending on the setting of the inverter output voltage. Since a sample of the 115 vac output is fed back through an output adjust potentiometer, R109, in the dc regulator, any variations in the output voltage or any adjustments in the voltage setting will be reflected in the oscillator's signal level. Two outputs are supplied by the oscillator; the first, a full wave rectified signal, which is applied to R113 feeding the Schmitt trigger in the pulser driver; the second, a half wave rectified signal, which is applied to switch Q106 in the inverter driver. The output level of the oscillator is variable from -4.4 to -7.0 volts, peak, and is controlled by oscillator regulator Q104. As the level of the 115 vac output or the setting of the output adjust potentiometer R109 varies, the emitter voltage supplied to oscillator Q105 varies inversely. Thus, if the 115 vac output increases, the rectified oscillator output voltage will decrease.

c. The phasing circuitry of the converter consists of the secondary of the phase A oscillator coil and the phases B and C coils. These three coils are connected in series, forming a three-sectioned secondary coil of the phase A oscillator. Therefore, phase A becomes the reference point for phases B and C. Each coil in the secondary forms a 60° phase shift of the 180° inversion of the phase A oscillator. The coil of the phase B oscillator (B26L101) forces the oscillator to oscillate with a phase difference of 120° (180° -60°) from the phase A reference oscillator. The phase C oscillator is forced to oscillate with a phase difference of 60° (180° - 120°) from the phase A reference oscillator. The physical connections of the phase C coil are reversed, thereby inverting the sine wave of phase C 180° which will produce the 240° phase shift required for phase C.

2-9. Pulser Driver

a. The pulser driver (fig. FO-3) consists of a Schmitt trigger, an overcurrent detector, and a summing circuit.

b. The pulser driver receives three inputs: a full wave rectified, 400 Hz oscillator signal, an overcurrent signal and a pulser feedback signal.

c, Operation of the pulser driver centers on the Schmitt trigger Q108-Q1O9, In quiescent conditions, Q108 will normally switch on and Q109 will switch off, which turns the pulser off. Primary control of the Schmitt trigger is provided by the oscillator's rectified

signal which is applied through summing resistor R113. Assuming that the Schmitt trigger has reached a quiescent condition, Q108 will be drawing sufficient base current to develop a +0.8 volt signal at its base and turn on Q109. Once Q109 is on, Q108 will turn off.

d. As the negative going oscillator signal is applied to Q108, the base voltage will drop to +0.6 volt turning Q108 off and turning on Q109. A negative going pulse output from Q109 will gate on the pulser and develop a feedback voltage across the charging capacitors at an initial rate of approximately 200 milivolts per microsecond. The feedback signal applied through summing resistors R113 and R114 will, for a no load condition, return Q108 to the quiescent state within a few microseconds. The Schmitt trigger requires approximately 20 microseconds to charge until Q108 begins to conduct once again and turn off Q109.

e. The Schmitt trigger will remain in the quiescent state until the oscillators negative input exceeds the pulsers positive feedback voltage at the base of Q108 by 0.2 volt, dropping the base of Q108 to +0.6 volt. Q109 will again turn on allowing the pulser to charge until the feedback voltage exceeds the oscillator voltage by 0.2 volt at the base of Q108.

f. Under no load conditions, the time it takes the Schmitt trigger to change states is quite long relative to the time it takes to change the integrator, therefore the integrator will charge to its full output within a few pulses.

g. Increasing the output load current will decrease the integrator charging rate and increase the amount of time it takes to charge the integrator to a voltage level which will turn on Q108. Therefore it will take a greater number of pulses or an increased duty cycle of the pulses, or both, to charge the integrator for this condition.

h. The overcurrent detector signal is a dc voltage that varies from +0.3 vdc (normal circuit operation) to -0.2 vdc (when output exceeds 2.5 times rated load). During normal system operation, the overcurrent detector Q112 will be in saturation. Should the output load exceed 1.5 times the rated load for a period of time longer than the time delay of the current limiting circuits, a negative going overcurrent signal will cut Q112 off and apply a +7 volt signal through isolation diode CR108 and summing resistor R114 to the base of Q108. This control voltage reduces the duty cycle of the Schmitt trigger output to a level that maintains the output load current at 1.5 times rated load. As described in the current limiting circuit description, paragraph 2-13, overloads in excess of 2.5 times rated load apply an immediate overcurrent signal to CR112 to limit the output current until the time delay circuit in the current limiting circuits time out.

i. The pulser feedback signal, which is developed at T1B center tap, varies with output voltage and load current requirements. This signal also exhibits a 1 to 3 volt ripple with a frequency of up to 20K hertz on the basic 20 to 32 volts, 400 Hz full wave rectified feedback signal. This ripple voltage is caused by the current pulsers which charge the integrator circuits on the pulser assembly.

j. The output of the pulser driver is a series of negative going pulse groups which drive the pulse amplifiers in the pulser circuit. The pulses swing from +28 volts to +0.4 volt and occur at a rate of 800 pulse groups a second with between 5 and 50 pulses in each group depending on output load.

2-10. Pulser

a. The pulser (fig. FO-2) gates current from the +28 volt supply and the input capacitor bank to the integrator circuit. The signal is applied to the center tap of the power transformer primary winding. The inverter circuit gates on alternate halves of the winding to generate a complete sine wave output in the secondary winding.

b. The pulser consists of a current switching network and a pulse integrator circuit which makes use, in part, of the power transformer T1. The pulser driver provides a group of negative going pulses, whose duty cycle varies with the voltage level of the 400 Hz oscillator signal and the output load current. The pulse groups are amplified by the pulse amplifiers Q5 and Q14, and applied to switches Q6 through Q8. Switches Q6-Q8 gate +28 volts to the integrator network consisting of L5, L6 and L7, C21, C22 and C23 and T1B. The integrator output, pin 6 of T1B, and alternate outputs of the inverted gate on section B of T1 primary winding. By so doing, a complete 115 vat, 400 ±7 Hz sine wave is generated in T1B secondary winding.

2-11. Inverter Driver

The oscillator circuit provides a half wave rectified sine wave to the inverter driver (fig. FO-3), where the signal is squared by switch Q106. The paraphase amplifier Q107 further shapes the square wave and provides two outputs 180 degrees out of phase to the switches Q110 and Q111. A current limiting sample is obtained from the junction of R125 and R126 in the summing circuit to maintain a constant current to the emitters of Q110 and Q111. Resistor R123 modifies the sample to eliminate effects of the inverter driver output on the feedback network. Resistor R120 provides dc bias to Q110 and Qlll.

2-12. Inverter

a. During normal operation, the pulser circuit applies a full wave rectified sine wave to the center tap of the power transformer T1B. In order to induce normal sine wave outputs in the secondary windings, alternate ends of the primary winding are gated to ground by

the inverter circuit (fig. FO-2). As an example, if T1B primary winding is gated to ground at pin 5 during the first half of the 400 Hz output, then pin 7 will be gated on during the second half cycle.

b. The output of the inverter driver is applied across the center tapped primary winding of current transformer T3. The output in the secondary winding is applied on alternate half cycles to current switches Q29, Q30 and Q31, or to Q20, Q21 and Q22. Assuming that switches Q29, Q30, and Q31 are turned on by a positive going pulse between pins 6 and 5 of T3, emitter current will begin to flow from pin 9 to 8 of T3 tickler winding and will induce a positive feedback signal in T3 secondary winding. This signal will drive Q29, Q30, and Q31 into saturation very quickly and will maintain that state until the pulse input from the inverter driver goes negative. On the second half of the cycle, a positive pulse will be applied to Q20, Q21 and Q22 which function in a similar manner.

c. Base resistors R19, R20, R21 feeding Q29-Q31 (R10, Rll, R12 for Q20-Q22) ensure that the drive current generated in the secondary of T3 is distributed equally among the base circuits. The output of Q29-Q31 is applied to pin 5 of power transformer T1B primary winding (Q20-Q22 is applied to pin 7). Diodes CR1l and CR14 protect Q20-Q22 and Q29-Q31 from inverse voltage spikes which may be generated in the pulse circuits under abnormal operating conditions in the output load or for loads exhibiting low power factors. Resistor R26, connected to the center tap of T3 secondary winding, develops the overcurrent signal which is an exact analog of the pulse current flowing in the inverter circuit. Capacitors C29 and C32 remove rf components from the inverter output pulse and aid the pulser integrator circuits in forming the output sine wave.

2-13. Current limiting Circuits

a. The current limiting circuits (fig. FO-3) consist of a current limit detector/time delay circuit and a summing circuit. The current limiting circuits monitor the output current and after a time delay, which is dependent upon the level of the overload, but no less than 5 seconds, reduce overloads in excess of 1.5 times rated full load current to no more than 1.5 times rated full load. The inverter is capable of operating continuously at 1.5 times its rated full load current.

b. For overloads in excess of 2.5 times rated full load, including short circuit loads, the biasing network in the summing circuit will be swamped and an immediate overload signal will be developed. This signal will turn off the pulser driver and hold it off until the pulse integrator circuit discharges sufficiently to drop the inverter output current to a value between 1.5 and 2.5 times rated full load (a period of approximately 20 to 40 microseconds). Since there are no buffering circuits acting at this point, the overload signal in the summing circuits will dissipate and the pulse driver will turn on again, causing overload currents to flow in the inverter once more. Again the summing circuits will be swamped and the overload protection cycle will be repeated.

c. As long as an overload in excess of 2.5 times rated full load exists, the summing circuits will alternately swamp and clear for approximately 5 seconds, after which time the current limit detector and time delay circuits will energize and apply a continuous overload control signal through the summing circuit to the pulse driver. This signal will then reduce the output current to 1.5 times rated full load for as long as the overload exists.

d. The overcurrent signal, obtained from current transformer T3, is applied to the base of the overcurrent delay amplifier Q113. The overcurrent signal varies from -0.4 volt, full rated load, to -10 volts, 2.5 times full rated load. Since Q113 collector voltage can vary from approximately + vdc to + 16.5 vdc (for example, saturation to cut off conditions), depending on the magnitude of the overcurrent signal; the voltage across the time delay control circuit of C109 and R129 will vary and cause the time delay introduced by the circuit to vary. The time delay introduced by this circuit varies from approximately 90 seconds for overloads slightly in excess of 1.5 times rated load to approximately 5 seconds for overloads in excess of 2.5 times rated load.

e. If an overload is removed before the delay circuit has energized, C109 will begin to discharge through R129. As a result, the time delay introduced by C109 and R129 will be shortened for second and subsequent overload applications. This shortening of the time in the time delay circuit is dependent on the severity of the overload and the periods of overload time versus normal load time.

f. During normal operation, Q113 will be conducting near saturation, thereby holding dc amplifier Q115 near cut off and dc amplifier Q114 near saturation. The delay overcurrent signal at the emitter of Q114 will be approximately +15.5 vdc. Referring to the summing circuit, the + 15.5 vdc signal will be applied across the voltage divider consisting of R125 and R126. The bias thus developed at the junction of R125–R126 adds algebraically with the -0.4 volt signal from T3-5 to produce a +0.3 vdc overcurrent signal to detector diode CR112 in the pulse driver circuit. Since Q112 is normally saturated, this signal has no effect on Q112, and the pulse driver circuit functions normally.

g. Overloads of 1.5 to 2.5 times rated load current will cause the overcurrent delay circuit to energize and apply a dc control voltage to Q115-Q114 which is proportionate to the level of the overload. The overcur-

rent signal from Q114 will also be proportionate to the overload, varying in the range of + 15.5 vdc to + 6 vdc. The lower the overcurrent signal from Q114, the lower the bias applied to R125 will be. The overcurrent signal at CR112 in the pulse driver will be between +0.3 vdc (normal load) and -0.2 vdc (2.5 times rated load). As this voltage drops below O volt, the overcurrent circuit in the pulse driver will turn off, limiting the inverter output to 1.5 times rated load.

h. When current loads sensed at pin 5 of transformers T2, T3 and T4 approach or exceed 2.5 times rated load, the overcurrent signal voltage is sufficiently negative to overcome the slightly positive bias normally developed at the junction of R125 and R126. As a result, the overcurrent circuit on the pulse driver is immediately cut off and the inverter output is reduced for 20 to 40 microseconds, as described previously. The overcurrent circuits will produce a cyclic type of current control until the time delay circuit energizes.

2-14. Output Power Transformer Circuitry

a. The output transformer circuit (fig. FO-2) consists of transformer T1B and capacitor C37. The transformer and capacitor combination form a tuned circuit at 400 Hz. Output distortion is controlled by capacitor C37. By selecting the proper capacitance value, approximately 13 microfarads, the output distortion can be regulated. Refer to paragraph 3-27 for the proper method of adjusting the output distortion.

b. In order to produce a 400 Hz sine wave signal in the secondary of Tl, pins 5 and 7 are gated off alternately by the inverter. The pulser generates a 400 Hz full wave rectified signal and applies it to pin 6, the center tap of T1's primary. By gating on alternate halves of the primary of T1, a 400 Hz sine wave is produced on the secondary.

c. The requirement for WYE or Delta operation of this inverter necessitates the use of the specially constructed transformer. There are three driven primaries, three output secondaries, and two tertiaries (third). The secondary of phase A is connected with the tertiaries to act as a pseudo or false tertiary. The tertiaries are connected in a Delta configuration to provide improved operation and phasing.

d. In addition, each secondary is paralleled with approximately 13 uf (C36, C37, and C38). This effectively forms an LC notch filter which eliminates frequencies other than the desired 400 Hz output. Despite rigid controls in manufacturing, there are still some differences between individual transformers which make it necessary to select the shunt capacitor for maximum reduction of unwanted harmonics.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

3-1. Voltage and Resistance Measurements

a. Table 3-1 shows the voltage and resistance measurements that can be expected in the inverter. Voltages were measured with no load on the output.

WARNING

Relatively low voltage but high current is present in the inverter.

b. Resistance measurements are shown in the forward and back mode. The resistance on the top indicates the forward resistance and the value on the bottom indicates back resistance.

Table 3-1. Voltage *and Resistance Measurements*

TEST CONDITIONS

A. Voltage measurements.

1. Input voltage + 28.0 vdc
2. Output voltage Adjust to 115.5 vac ±0.5 vac 400 Hz No Load.
3. Voltage listing Voltages are referenced to ground.

NOTE

The figure number in the voltage columns indicate the figure in which the wave form is shown.

B. Resistance measurements.

1. All resistance measurements are ±2%.
2. Remove associated Z elements indicated by* .

REFERENCE DESIGNATION	VOLTAGE/WAVE FORM			RESISTANCE	
	E	B	C	C-B	E-B
A1Q5, Q9, Q1*	28 vdc	Fig FO-1	Fig. FO-1	4 15K	10 15K
AlQ2 thru 4*	Fig. FO-1	Fig. FO-1	28 vdc	3 20K	10 15K
A1Q6 thru 8*	Fig. FO-1	Fig. FO-1	28 vdc	3 20K	3 20K
A1Q1O thru 12*	Fig. FO-1	Fig. FO-1	28 vdc	3 20K	3 20K
A1Q13, Q14, Q15	28	Fig. FO-1	Fig. FO-1	5 15K	5 200
B26Q104	9.3	10	17	7 5K	7 15K
B26Q105	Fig. 3-7	Fig. 3-7	Fig. FO-1	l00K 7	l00K 7
B26Q106	0	Fig. 3-5	Fig. FO-1	7 l00K	7 l00K
B26A107	Fig. 3-5	Fig. FO-1	Fig. FO-l	7 7K	7 7K
B26Q108	0	0	Fig. FO-1	7 8K	7 3.5K
B26Q109	0	Fig. 3-5	Fig. 3-5	7 6K	7 3K
B26Q110	Fig. 3-5	Fig. 3-5	Fig. 3-5	5 *a*	5 16
B26Q111	Fig. 3-5	Fig. 3-5	Fig. 3-5	5 *a*	5 40
B25Q112	0	Fig. 3-3	Fig. 3-3	7 3K	7 3K
B26Q113	0	0	0	7 100K	7 l00K

Table 3-1. Voltage and Resistance Measurements–Continued

REFERENCE DESIGNATION	VOLTAGE/WAVE FORM			RESISTANCE	
	E	B	C	C-B	E-B
				7	7
B26Q114	15	15.7	17	4K	9K
				7	7
B26Q115	5.3	6.0	15.7	30K	30K
				4	4
B28Q16	16.5	17	28	10K	8K
				6	6
B25Q1, Q101	0	0	16	18K	20K
				7	7
B25Q2, Q102	0	Fig. 3-3	Fig. 3-3	18K	4K
				7	7
B25Q3, Q103	0	0	Fig. FO-1	3K	3K
				7	7
B25Q4, Q104	Fig. 3-7	Fig. 3-7	Fig. FO-l	200K	200K
				5	5
B25Q5, Q105	Fig. 3-5	Fig. 3-5	Fig. 3-5	*a*	5K
				7	7
B25Q6, Q106	Fig. 3-5	Fig. FO-l	Fig. FO-1	5K	8K
				7	7
B25Q7, Q107	0	Fig. 3-5	Fig. FO-l	l00K	l00K
				7	7
B25Q8, Q108	6.8	7.5	9	9K	7K
				6	6
B25Q9, Q109	Fig. 3-5	Fig. 3-5	Fig. 3-5	600K	20
				6	6
B25Q10, Q110	8.3	9.0	17	2.5K	18K
				7	7
B26Q101	19	19.7	28	2K	6K
				5	5
B26Q102	17	17.7	28	3K	5K
				6	6
B26Q103	6.8	7.5	10	2K	6K

3-2. Circuit Waveforms

Figure FO-1, detailed block diagram, shows the waveforms that can be expected in the inverter. Waveforms on all three phases are identical. Table 3-2 has been provided to reference the components listed in the block diagram (phase A) to the corresponding components in phases B and C.

Table 3-2. Component Reference

PHASE A	PHASE B	PHASE c	PHASE A	PHASE B	PHASE c	PHASE A	PHASE B	PHASE c
R101	.....	.....	R136	R107	R7	L101	L101	L1
R102	.....	.....	R137	.....	.....	Q101	.....	.....
R103	.....	.....	R138	.....	.....	Q102	.....	.....
R104	R125	R25	R139	.....	.....	Q103	Q108	Q8
R105	R120	R20	R140	.....	.....	Q104	Q11O	Q1O
R106	R106	R6	R141	.....	.....	Q105	Q104	Q4
R107	R119	R19	R142	.....	.....	Q106	Q107	Q7
R108	R105	R5	CR101	.....	.....	Q107	Q106	Q6
R109	R101	R1	CR102	.....	.....	Q108	Q103	Q3
R11O	R124	R24	CR103	.....	.....	Q109	Q102	Q2
R111	R113	R13	CR104	.....	.....	Q110	Q109	Q9
R112	R123	R23	CR105	CR108	CR8	Q111	Q105	Q5
R113	R112	R12	CR106	CR104	CR4	Q112	Q101	Q1
R114	R104	R4	CR107	CR106	CR6	Q113	.....	.....
R115	R111	R11	CR108	CR103	CR3	Q114	.....	.....
R116	R122	R22	CR109	CR107	CR7	Q115	.....	.....
R117	R117	R17	CR11O	CR11O	CR1O			
R118	R118	R18	CR111	CR109	CR9			

Table 3-2. Component Reference–Continued

PHASE A	PHASE B	PHASE C	PHASE A	PHASE B	PHASE C	PHASE A	PHASE B	PHASE C
R119	R110	R10	CR112	CR102	CR2			
R120	R116	R16	CR113	CR105	CR5			
R121	R109	R9	CR111	.....	.....			
R122	R103	R3	C101	.....	.....			
R123	R115	R15	C102	C107	C7			
R124	R108	R8	C103	C104	C4			
R125	R121	R21	C104	C106	C6			
R126	R114	R14	C105	.....	.....			
R127	.....	.....	C106	C105	C5			
R128	.....	.....	C107	C108	C8			
R129	.....	.....	C108	C109	C9			
R130	.....	.....	C109	.....	.....			
R131	.....	.....	C110	.....	.....			
R132	.....	.....	C111	C101	C1			
R133	.....	.....	C112	C103	C3			
R134	.....	.....	C113	.....	.....			
R135	.....	.....	C114	.....	.....			

NOTE

Prefix all Phase A reference designations with B26. Prefix all Phases B and C reference designations with B25.

PHASE A	PHASE B	PHASE C	PHASE A	PHASE B	PHASE C
Q1	Q5	Q9	CR2	CR5	CR8
Q2	Q6	Q10	CR3	CR6	CR9
Q3	Q7	Q11	L2	L5	L8
Q4	Q9	Q12	L3	L6	L9
Q13	Q14	Q15	L4	L7	L10
Z1	Z2	Z3	C18	C21	C24
Z4	Z8	Z11	C19	C22	C25
Z5	Z9	Z12	C20	C23	C26
Z6	Z10	Z13	R1	R2	R3
CR1	CR4	CR7	R4	R5	R6

NOTE

All reference designations in the above table have a prefix of Al.

PHASE A	PHASE B	PHASE C	PHASE A	PHASE B	PHASE C
Q17	Q20	Q23	R16	R19	R22
Q18	Q21	Q24	R17	R20	R23
Q19	Q22	Q25	R18	R21	R24
Q26	Q29	Q32	R25	R26	R26
Q27	Q30	Q33	CR10	CR11	CR12
Q28	Q31	Q34	CR13	CR14	CR15
R7	R10	R13	C28	C29	C30
R8	R11	R14	C31	C32	C33
R9	R12	R15	T2	T3	T4

NOTE

All reference designations in the above table have a **prefix** of A2.

Section II. TOOLS AND EQUIPMENT

3-3. Test Equipment

Common types of test equipment, considered as normal general support inventory items, are used on the maintenance and test of the inverter. These items are listed in table 3-3. This equipment is required but is not supplied with the inverter. Substitution of equipment as listed in table 3-3 is authorized if substitute equipment is of the same quality as the original equipment noted.

Table 3-3. Test Equipment Required

Item	Nomenclature Part Number	National/NATO Stock Number	Qty
Oscilloscope	AN/USM-281	6625-00-228-2201	1
Digital Voltmeter	AN/GSM-64	6625-00-165-5779	3
Voltmeter	ME-30	6625-00-643-1670	1
Counter	AN/USM-207	6625-00-044-3228	1
Distortion Analyzer	TS-723A	6625-00-668-9418	1
Multimeter	AN/USM-223	6625-00-999-7465	1
Tool Kit, Electronic Equipment	TK-100	5180-00-605-0079	1
Tool Kit, Electronic Equipment	TK-101	5180-00-064-5178	1

Table 3-4. Additional Equipment Required

ITEM	DESCRIPTION	MANUFACTURER	QTY
Test Fixture			
Variac		Staco Type 501	3
Resistor	0.1 ohms 100W Calibrated		3
Resistor	0.01 ohms 100W Calibrated	Commercial	3
Switch (S3)	4 Pole 3 Position, 5 amp	Commercial	1
Switch (S-4)	3 Pole 3 Position, 5 amp		
Switch (S-2)	3 Pole 2 Position, 5 amp	Commercial	1
Switch (S-5)	1 Pole 4 Position, 2 amp	Commercial	1
Load (+.75)	Resistor 55.7 ± 1% 250W; Capacitor 2.3 uf ± 3%	Commercial	3
Load (−.95)	Resistor 70.6 ± 1% 250W; Inductor 28.5 mh ± 3%	Commercial	3
Load (+1.0)	Resistor 52.9 ± 1% 250W	Commercial	3
Relay	4 Pole 2 Position 120 vac	Commercial	3
Connector	Ms3106F-22-6S	Cannon	1
Connector	MS3106F-22-5P	Cannon	1
Switch (S6)	3 Pole single throw momentary contact, 10 amp	Commercial	1
Switch (S1)	3 Pole 2 Position, 5 amp	Commercial	1
Capacitor			
4.0 uf 150 vac		Commercial	6
2.0 uf 150 vac		Commercial	3
1.0 uf 150 vac		Commercial	3
0.5 uf 150 vac		Commercial	3
Switch	SPST		15

Section III. TROUBLESHOOTING

3-4. General

a. Since there are no external controls or indicators on the inverter, performance indications maybe measured with the inverter disassembled on the test bench. While voltages in the inverter are relatively low (that is, +28 vdc and 115 vat), current levels are high (up to 45 amperes in normal operation, and much higher in short circuit situations where the input capacitor bank can discharge through the short). Failures may be self-evident; therefore, voltages should not be applied to the unit until it has been opened and visually inspected for burned or otherwise damaged components. Where failed components are located, resistance and continuity check should be performed to isolate the faulty circuits and to identify the cause of the failure. It will be necessary to remove protective coating from leads to take readings,

b. Troubleshooting will be performed with the inverter disassembled as necessary. Connect the test fixture shown in figure FO-6.

c. Once the cause of the malfunction has been determined and corrected, ensure that the defective component was the cause of the problem and not the result of another defective component.

Table 3-5. Symtom Diagnosis Chart

Malfunction	Possible cause	Corrective action
1. No output (low input current)	*a.* Open connection at: (1) A1L1 (2) B1200 capacitor assembly (3) B28Q16 (4) B26E4 or B26EJ (5) Between B26Q16 at T2-2	*a.* Check and repair.
	b. Open or shorted components: (1) B26Q102, B28Q16, B26Q101 open. (2) B26CR102, B26CR103 shorted.	*b.* Regulator defective. Refer to paragraph 3-12.
2. Excessive input current (current greater than 10 amp when voltage is less than 1 volt)	+ 28 vdc input shorted.	Refer to paragraph 3-11 or paragraph 3-16.
3. Excessive input current (input current greater than 15 amp when input voltage is between 5 and 7 volts)	*a.* Short in output. *b.* Short in pulser. *c.* Short in inverter.	*a.* Refer to paragraph 3-22. *b.* Refer to paragraph 3-16. *c.* Refer to paragraph 3-18.

3-5. Troubleshooting Procedure

a. Paragraphs 3-6, 3-7, and 3-8 give procedures for determining the cause of no input current, low input current and high input current in the inverter.

b. Table 3-5 is an aid in localizing a malfunction to circuit level. References have been made in the table to the detailed troubleshooting paragraph applicable to the specific circuit under test.

c. Table 3-6 troubleshooting guide has been prepared to aid in the isolation and repair of specific malfunctions that may occur in the inverter.

3-6. Procedure for Determining Cause of No Input Current

a. Visually check for broken wiring.

b. Apply+ 28 vdc to J1.

c. Measure voltage at pin 13 of A5 (fig. FO-2). (Voltage shall equal input voltage.)

(1) If voltage is present, proceed to *d* below.

(2) If voltage is not present:

(a) Check input cable.

(b) If cable checks good, replace filter A5.

d. Measure voltage at collector of B28Q16. (Voltage shall equal input voltage.)

(1) If voltage is present, proceed to *e* below.

(2) If voltage is not present, replace wire between B28E8 and L1-2.

e. Measure voltage at B26E4. (Voltage shall equal input voltage.)

(1) If voltage is not present, replace wire between B26E4 and B28E8.

(2) If voltage is present, troubleshoot regulator (para 3-12).

3-7. Procedure for Determining Cause of Low Current

a. Apply +28 vdc to J1.

b. Measure voltage at L1-1 (fig. FO-2). (Voltage shall equal input voltage.)

(1) If voltage is present, proceed to *c* below.

(2) If voltage is-not present, check input cable. If voltage is present on cable, replace filter A5.

c. Measure waveform at:

Anodes of B26CR110 and B26CR111 (fig. 3-7 and table 3-2).

Anodes of B25CR110 and B25CR111 (fig. 3-7 and table 3-2).

Anodes of B25CR10 and B25CR11 (fig. 3-7 and table 3-2).

(1) If any of the above voltages are not correct, proceed to *d* below.

NOTE

This procedure is written assuming phase A has malfunctioned. Refer to table 3-2 for corresponding component designations for phases B or C.

(2) Current shall rise to 10 amperes between +15 and +16 vdc, then drop to between 4 to 6 amperes at 28 vdc. If current exceeds these values, proceed to paragraph 3-8.

d. Measure voltage at the base of B28Q16 (fig. 3-2).

(1) If voltage is correct, proceed to *e* below.

(2) If voltage is not correct, troubleshoot regulator (para 3-12).

e. Measure waveform at collector of B26Q106 (fig. 3-7).

(1) If waveform is correct, troubleshoot driver (para 3-17).

(2) If waveform is not correct, proceed to *f* below.

f. Measure waveform at collector of B26Q105 (fig. FO- 1). If waveform is correct, troubleshoot oscillator (para 3-13).

g. Disconnect wire between L1-2 and input capacitor bank.

h. Troubleshoot capacitor bank (para 3- 11).

i. Reconnect wire between L1 -2 and input capacitor bank.

j. Apply +28 vdc to connector J1.

k. Measure voltage at B26Q109 collector (fig. 3-5). If waveform is not within limits, proceed to *l* below (fig. 3-5).

l. Troubleshoot pulser driver (para 3-15). If pulser driver checks good, proceed to *m* below.

m. Measure voltage at collector of B26Q105 (fig. FO-1).

(1) If voltage is correct, troubleshoot oscillator (para 3- 13). (See *o* below).

(2) If voltage is not correct at the collector of B26Q105, measure voltage at T1-B-6. If either voltage is correct, troubleshoot summing network (para 3-20).

n. If oscillator checks good, troubleshoot regulator (para 3-12).

o. Measure waveform at anodes of B26CR110 and B26CR111 (fig. 3-7).

(1) If waveforms are not within limits, proceed to *q* below.

(2) If waveforms are within limits, proceed to *r* below.

p. Trouble oscillator (para 3-13).

q. Troubleshoot inverter driver (para 3-17).

r. Turn off power supply and adjust to 0 volt.

s. Slowly increase voltage to inverter, while observing input current.

3-8. Procedure for Determining Cause of High Input Current

NOTE

This procedure was written assuming phase A has malfunctioned. Refer to table 3-2 for corresponding reference designations for phases B and C.

a. Visually check for damaged components.

b. Disconnect pulser lead at T1B pin 6.

c. Measure resistance from B26E2 (fig. FO-2) to the wire which connects with T1B pin 6.

(1) If resistance is infinite, troubleshoot pulser (para 3-16).

(2) If resistance is not infinite, proceed to *d* below.

d. Reconnect pulser lead to T1B pin 6.

e. Disconnect leads from T1B pins 5 and 7 (fig. FO-2).

f. Measure resistance from T1B pin 5 to A2T2 pin 8 and T1B pin 7 to A2T2 pin 8 (fig. FO-2).

(1) If resistance is infinite at either location, troubleshoot inverter (para 3-18).

(2) If resistance is not infinite, proceed to *g* below.

g. Reconnect leads to T1B pins 5 and 7.

(1) If input current is excessive and pulser output voltage is not low, check voltage at B26E9.

(2) If voltage is low, troubleshoot inverter (para 3-18).

h. If current is still excessive, troubleshoot output padding caps (A27C37) (fig. FO-3).

(1) If output padding caps are defective, replace.

(2) If output padding caps are good, proceed to table 3-5.

3-9. Procedure for Determining Cause of Unregulated Output Voltage

a. Visually check unit for burned components.

b. Slowly increase input voltage to inverter to +28 vdc while observing input current.

NOTE

Current will rise to 10 amperes between 15 and 16 vdc, then drop to between 4 to 6 amperes at +28 vdc. If current exceeds these values, proceed to paragraph 3-8.

c. Check waveform at B26E1 (fig. FO-1).

(1) If waveform is within limits, troubleshoot pulser (para 3-16).

(2) If waveform is not within limits, proceed to *d* below.

d. Check waveform at collector of B26Q108 (fig. 3-5).

(1) If waveform is within limits, troubleshoot pulser driver (para 3-15).

(2) If waveform is not within limits, proceed to *e* below.

e. Check waveform at collector of B26Q105 (fig. FO-1).

(1) If waveform is within limits, troubleshoot oscillator (para 3- 12).

(2) If waveform is not within limits, troubleshoot oscillator regulator (para 3-12).

Table 3-6. Troubleshooting Guide

Item of Check	Test Conditions	Test Equip. Connection	Test Equip. Reference	Normal Readings	Paragraph Reference
Input Filter	+28 vdc in no load	L101-1	Note 1	+28 vdc	3-10
Series Reg.	+28 vdc in no load	Q16-E	Note 1	+16 vdc	3-12
Series Reg.	+28 vdc in no load	B26Q102-E	Note 1	+16.5 vdc	3-12
Oscillator	+28 vdc in no load	B26Q105-C	Note 2	400 Hz sine wave	3-13
Oscillator	+28 vdc in no load	B26CR105 Anode	Note 2	400 Hz half wave rec	3-13
Oscillator	+28 vdc in no load	CR107 Anode	Note 2	400 Hz full wave rec	3-13
Inverter Driver	+28 vdc in no load	B26CR110 Anode	Note 2	400 pps square wave	3-17
Inverter	+28 vdc in no load	A2CR11 Cathode	Note 2	400 Hz pos. pulse	3-18
		A2CR14 Cathode	Note 2	400 Hz pos. pulse	3-18
Pulser Driver	+28 vdc in no load	B26Q109-C	Note 2	+28 V P-P pulse groups	3-15
Pulser	+28 vdc in no load	T1-B-6	Note 2	800 Hz pos. pulse	3-16

NOTE

1. Volts/CM 0.5 V/CM
   HORZ/Sweep 0.5 MS/CH
   Mode dc
   Sinc Internal
2. Volts C/M 1.0 V/CM
   HORZ/Sweep 0.5 MS/CM
   Mode dc
   Sine Internal
3. All waveforms are shown on the detailed block diagram (fig. FO-1).

Table 3-7. Troubleshooting Chart

CAUTION

When troubleshooting, slowly increase input voltage from 0 to +28 vdc. Do not apply instantaneously. Input current shall increase to 10 amperes at +15 to +16 vdc, then drop to 4 to 6 amperes at +28 vdc.

NOTE

Improper operation of one phase will cause similar symptoms on the other two phases.

Malfunction	Possible cause	Corrective action
1. No output (very low input current)	*a.* Open connections at: (1) A1L1 (2) B1200 Capacitor Assembly (3) B28Q16 (4) B26E4 or B26E5	*a.* Rework connections as required.
	b. The following components open or shorted (1) B26Q102 open (2) B28Q16 open (3) B26Q101 open (4) B26CR102 or B26CR103 shorted	*b.* Use multimeter to check components, replace as necessary.
	c. Open between B28016 Emitter and T2-2.	*c.* Check continuity and repair if necessary.
2. Excess input current: (current greater than 10 amps when voltage is in less than 1 volt)	*a.* Shorted components: A1-Q2, 3, 4 Q6, 7, 8 Q10, 11, 12 A1-CR1, 2, 3 CR4, 5, 6 CR7, 8, 9	*a.* Check components and replace if defective **NOTE** Refer to table 3-1 for voltage and resistance values.

NOTE

Replace transistor(s) and associated Z element(s) if transistor or Z element(s) are defective. Replace all three transistors in a phase grouping if one transistor is defective.

NOTE

Before checking transistors remove Z element and emitter connections.

	b. Shorted input capacitators in input capacitator bank.	*b.* Disconnect connection at L1-2, measure resistance with positive lead of multimeter on capacitor bus to chassis. Resistance shall be high (greater than 50K ohms).

Table 3-7. Troubleshooting Chart-Continued

Malfunction	Possible cause	Corrective action
3. Excessive input current. (Input current is greater than 15 amps when voltage in is approximately 5 to 7 volts.)	*a.* Shorted components: A26Q110 and Q111 A25Q105 and Q109 A25Q5 and Q9 A25C1 and C101 A26C112	*a.* Check with multimeter and replace as necessary.
	b. Shorted power switch transistors (A2Q17 through A2Q34).	*b.* Isolate to one phase group by measuring resistance with positive lead on transformers T1A, B and C pins 5, 6, 7 and negative lead on chassis. Resistance shall be greater than 20K ohms in this configuration. **NOTE** With leads reversed resistance will be approximately 15 ohms.
	c. Diodes A2CR10 through A2CR15 shorted.	*c.* Check with multimeter and replace as necessary.
	NOTE Open collector or cathode connections as necessary to measure individual components.	
	d. Output shorted to chassis ground.	*d.* Check J2 pins for following values: J2-A - 8.4K (See note below) B - Infinite C - Infinite D - Infinite (See note below) E - Infinite F - Infinite **NOTE** Remove connection from T1B-1. If different values are recorded, refer to paragraphs 3-21 and 3-22.
	e. Shorted components. (1) Capacitors on A27 module. (2) B28T5 or T6 (3) Input/output filter	*e.* Check with multimeter and replace as necessary.
	f. A1C18-A1C26 shorted.	*f.* Remove positive lead of capacitors and check with multimeter. Replace as necessary.
4. Unit operates with correct output voltage but distortion is greater than 6% under all load conditions.	*a.* Pulser driver not operating.	*a.* Refer to paragraph 3-15.
	b. Inadequate drive.	*b.* Check signals at A1Q1, Q5 and Q9 collectors. Voltages shall approximate the input voltage. If voltage is less than ⅔ the input voltage, replace transistor and Z element.
5. Distortion greater than 7% on one or two phases.	*a.* Improper drive signals at: (1) B25E14 and E15 (2) B25E4 and E9 (3) B26E1 and E9	*a.* Refer to figure 3-7 and paragraph 3-17.
	b. Capacitors A27C36, A27C37, or A27C38 open.	*b.* Check with multimeter and replace as necessary.
6. Excess distortion (5 to 7%) on all phases.	*a.* Pulser drive inbalance.	*a.* Remove B25R111 and substitute a decade resistance box. Adjust resistance as necessary, but not less than 43K ohms for proper performance.
	NOTE If padding caps are balanced, adjust B25R111 for best performance then adjust padding caps (A27C36, A27C37, A27C38). If capacitors are within 1 microfarad of each other they are considered balanced.	
	b. See step 6 of this chart.	*b.* See step 5.
	c. Shortened windings in transformer T1.	*c.* Replace transformer.

Table 3-7. Troubleshooting Chart-Continued

Malfunction	Possible cause	Corrective action
		NOTE Shorted transformer windings cannot be detected with normal test equipment. Exhaust all other procedures before replacing T1.
7. Output voltage does not regulate.	*a.* Feedback circuit open.	*a.* Replace broken wires in feedback circuit (fig. FO-1).
	b. No signal at:	*b.* Check the following if no signal is present at:
	B25E6	B25E6 - B28U28 open B26T6 open
	B25E16	B25E16 - B28U28 open B28T5 open
	B26E6	B26E6 - B28R31 open A1R29 shorted
	c. No voltage feedback to B26E7, B25E12, B25E2.	*c.* Refer to paragraphs 3-19, 3-20, and 2-13.
	d. Drive regulator bad.	*d.* Refer to paragraph 3-12.
8. Output voltage too low.	*a.* Unit in current limit mode.	*a.* Refer to paragraph 3-20 and check overcurrent detector B26Q112, B25Q101 and Q1 for an open.
	b. Current sense resistors open (R25, R26, R27 on A2).	*b.* Replace if defective.
	c. Transformers A2T2, A2T3, A2T4, ground bus bad.	*c.* Refer to paragraph 3-20*d*.
9. Unit will not limit with output overload.	*a.* Current sense circuit.	*a.* Refer to paragraph 3-20*d*.
	b. Defective summing circuit.	*b.* Refer to paragraph 3-19.
10. Outputs out of phase.	*a.* Oscillators not wired correctly.	*a.* Check connections at B26E18, B26E19, B25E18, B25E19.
	b. B26L101 open.	*b.* Check with multimeter and replace as necessary.
	c. Defective components or connections: B28R28 B28R30 B28C27 B25E20	*c.* Check and replace or correct as necessary.
11. Unit not operating at correct frequency.	*a.* Oscillator out of adjustment.	*a.* Refer to paragraph 3-24.
	b. Oscillator adjust caps defective. B26C104	*b.* Check capacitor and replace as per paragraph 3-24.

3-10. Input Filter

a. Nominal +28 vdc is applied through pins A and C of input connector J1 to the low pass input filter (fig. FO-2). Input to the filter is variable, from +26 vdc to +29 vdc, and is capable of supplying load currents of up to 41 amperes. Capacitors A5C501 and A5C502 shunt high frequency noise generated either by external or internal sources to ground. Inductor A5L501 is a high frequency choke which presents a high impedance to voltage spikes and rf impulse noise that may be present on the +28 vdc bus. The +28 vdc output from the input filter is applied to the +28 vdc bus, where it is distributed to the pulser circuits.

NOTE

The input filter is an encapsulated pairable module.

3-11. Input Capacitor Bank

a. Check for open or shorted capacitors with an ohmmeter. Replace any open or shorted capacitors (fig. 3-1 and FO-2).

3-12. Regulator

a. Apply +28 vdc to inverter and check voltage at B26E5. Voltage shall be + 16.6 vdc + 0.5 volt.

b. If voltage is not + 16.6 vdc, turn off power supply and troubleshoot series regulator as follows:

(1) Check for open or shorted transistors B26Q101, Q102; resistors B26R101, R103, R104, R137, R138; zener diodes B26CR102, CR103, CR104. Replace any open or shorted components.

(2) If components are not defective, apply +28 vdc to inverter and check with an oscilloscope, for

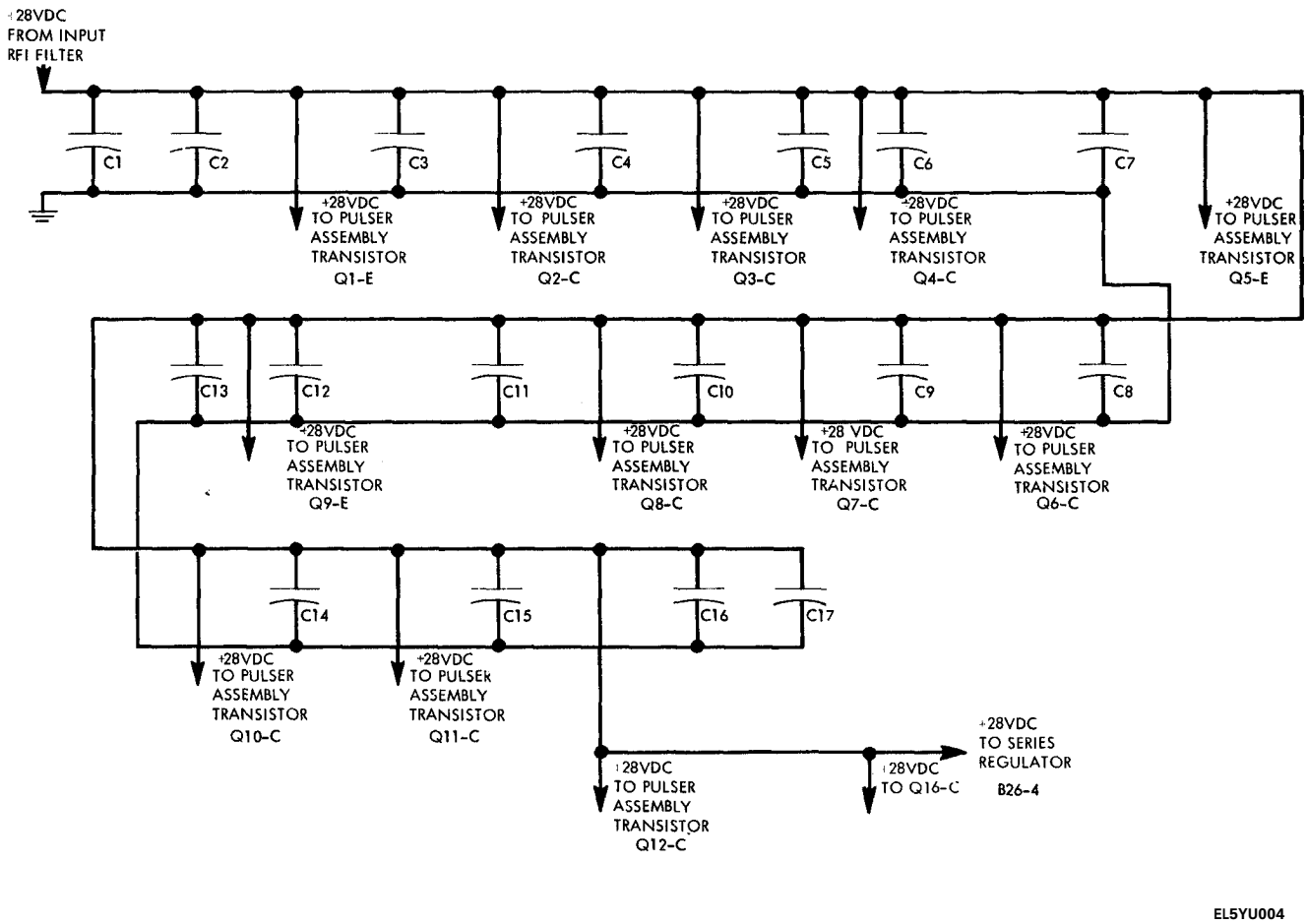


Figure 3-1. Input Capacitor Bank Detailed Schematic Diagram.

zener diodes B26CR102, CR103 or B26CR104 breaking down. (Turn off power supply and set output voltage to 0 volt.) Replace any diode that is breaking down.

c. If input current is excessive, troubleshoot inverter in accordance with paragraph 3-18. Input current shall increase to 10 amperes at +15 to +16 vdc, then drop to 4-6 amperes at +28 vdc. Do not allow input current to exceed these values.

d. Check for open or shorted transistors B26Q103, Q104; capacitors B26C101, C102, C105, C113; diode B26CR101, potentiometer B26R109, and resistors B26R140, R107, R102, R139, R106 (fig. 3-2), using an ohmmeter. Replace any open or shorted components.

e. If components are not defective, apply +28 vdc to inverter and check with an oscilloscope for diode B26CR101 or B26CR114 breaking down. Turn off power supply and replace diode if breakdown is indicated.

3-13. Oscillator Phase A

a. Check for open or shorted transistor B26Q1O5 capacitors B26C103, C104, C106; diodes B26CR1O5 CR106, or resistors B26R107, R108, R111, using a ohmmeter. Replace any open or shorted component (fig. 3-3 and 3-16).

b. If no components indicate open or short, appl +28 vdc to inverter and check with an oscilloscope for diodes B26CR105, CR106, or CR107 breaking down Turn off power supply and set output voltage to volts. Replace any diodes that are breaking down.

c. If no components are open or shorted and diodes are not breaking down, replace inductor B26L101.

d. Check and adjust output frequency in accordance with paragraph 3-25.

e. Check phasing with oscilloscope in accordance with timing diagram, figure 3-4.

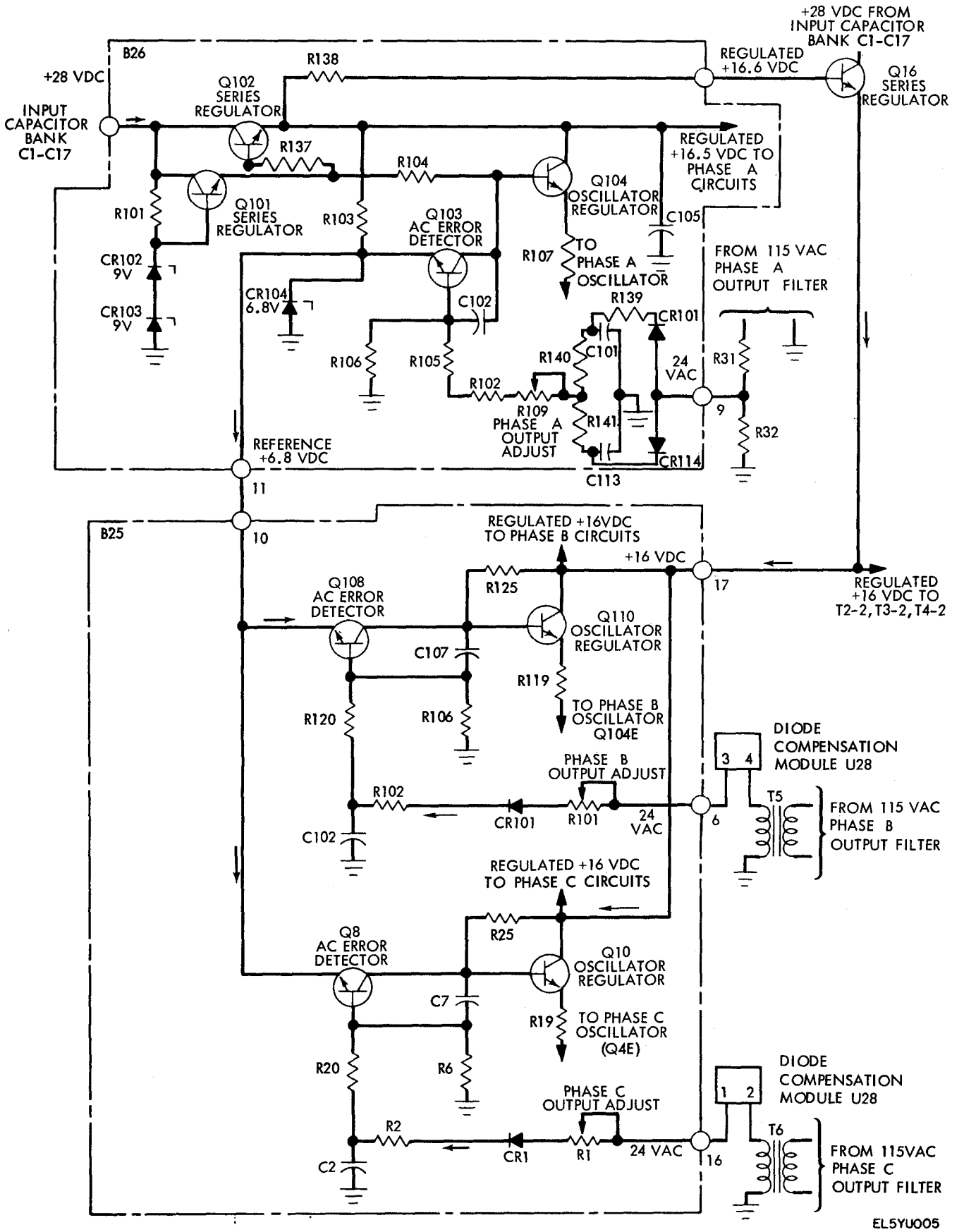


Figure 3-2. Regulator Detailed Schematic Diagram.

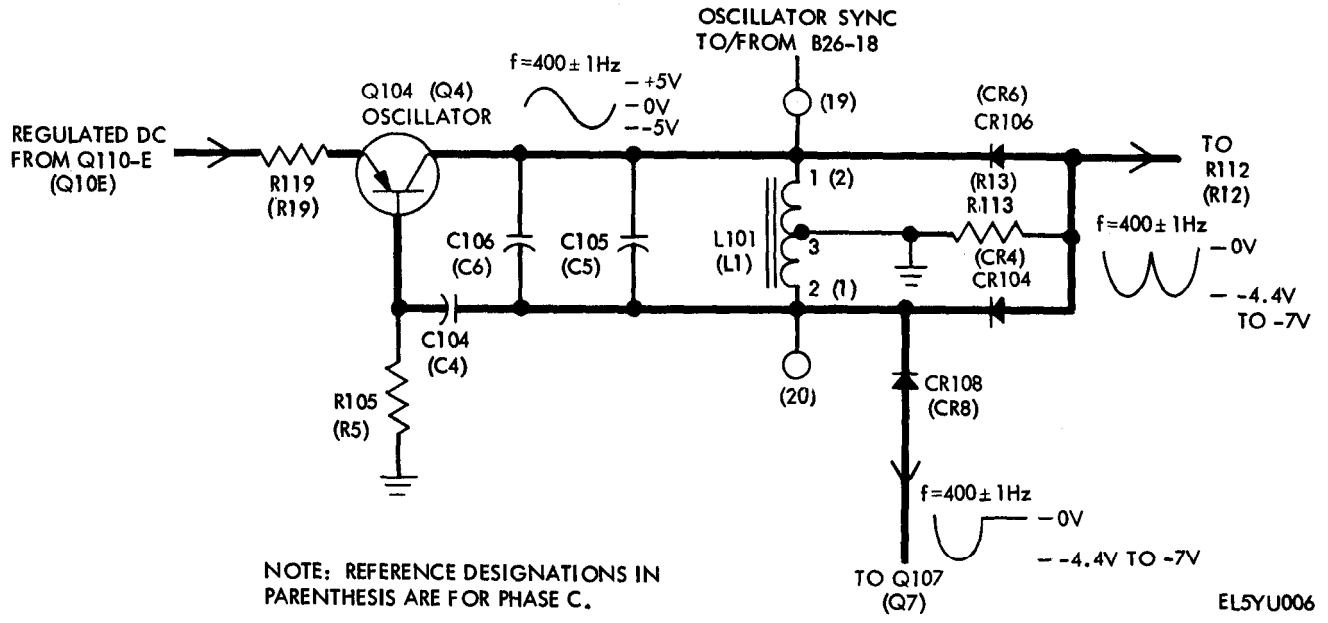


Figure 3-3. Oscillator Detailed Schematic Diagram.

3-14. Oscillator Phases Band C

Refer to paragraph 3-13 for troubleshooting procedure and table 3-2 for reference designations.

3-15. Pulser Driver

a. Check for open shorted transistors B26Q108, Q109, and Q112; capacitors B26C112, C111; diodes B26CR108, CR112; and resistors B26R113, R114, R115, R119, R121, R124, R122, using an ohmmeter. Replace any open or shorted components.

b. If no components indicate open or shorted, apply +28 vdc to inverter and check with an oscilloscope for diodes B26CR108 or B26CR112 breaking down. Turn off power supply and set output voltage to 0 volts. Replace any diode that is breaking down.

c. If input current is excessive, turn on power supply. Slowly, increase output voltage of power supply while observing input current. Input current shall increase to 10 amperes at +15 to +16 vdc, then drop to 4-6 amperes at +28 vdc. Input current shall not exceed these values. If input current is excessive, troubleshoot inverter in accordance with paragraph 3-18.

3-16. Pulser

a. If distortion is noted in the output, check for open or shorted capacitor A1C37 with an ohmmeter. Replace shorted or open capacitor A1C37 and perform output distortion check and adjustment in accordance with paragraph 3-27.

b. If input current is excessive, troubleshoot pulser as follows:

(1) Remove nuts and lugs from transistor A1Q5 through A1Q14 (fig. 3-14, sheet 2). Disconnect lead from terminal 6 of transformer T1B.

(2) Check each circuit for open or shorted transistors, diodes, Z elements and inductors using an ohmmeter (fig. 3-6 and table 3-l).

(3) Once defective circuit or circuits are determined, determine which component or components are defective and replace those components.

3-17. Inverter Driver

a. Apply +28 vdc to inverter and check voltage at collector of switch transistor B26Q106 (fig. 3-7), with an oscilloscope. Voltage shall be as shown in figure FO-1. If voltage is not as shown, turn off power sup ply and check for open or shorted transistors B26Q106 (fig. 3-7 and 3-16) or open or shorted resistors B26R110, B26R112, B26R116, using an ohmmeter.

b. Measure voltages at the collectors of push-pull amplifier, transistors B26Q110, B26Q111, Voltage shall be as shown in figure 3-7 and 180 degrees out of phase. If voltages are not as shown, turn off power supply and check for open or shorted transistor B26Q110, B26Q111 (fig. 3-7 and 3-16), capacitor B26C107, diode B26CR109 and resistors B26R116 B26R117, R118, R120, R123,

c. If voltages are within limits at the collectors of

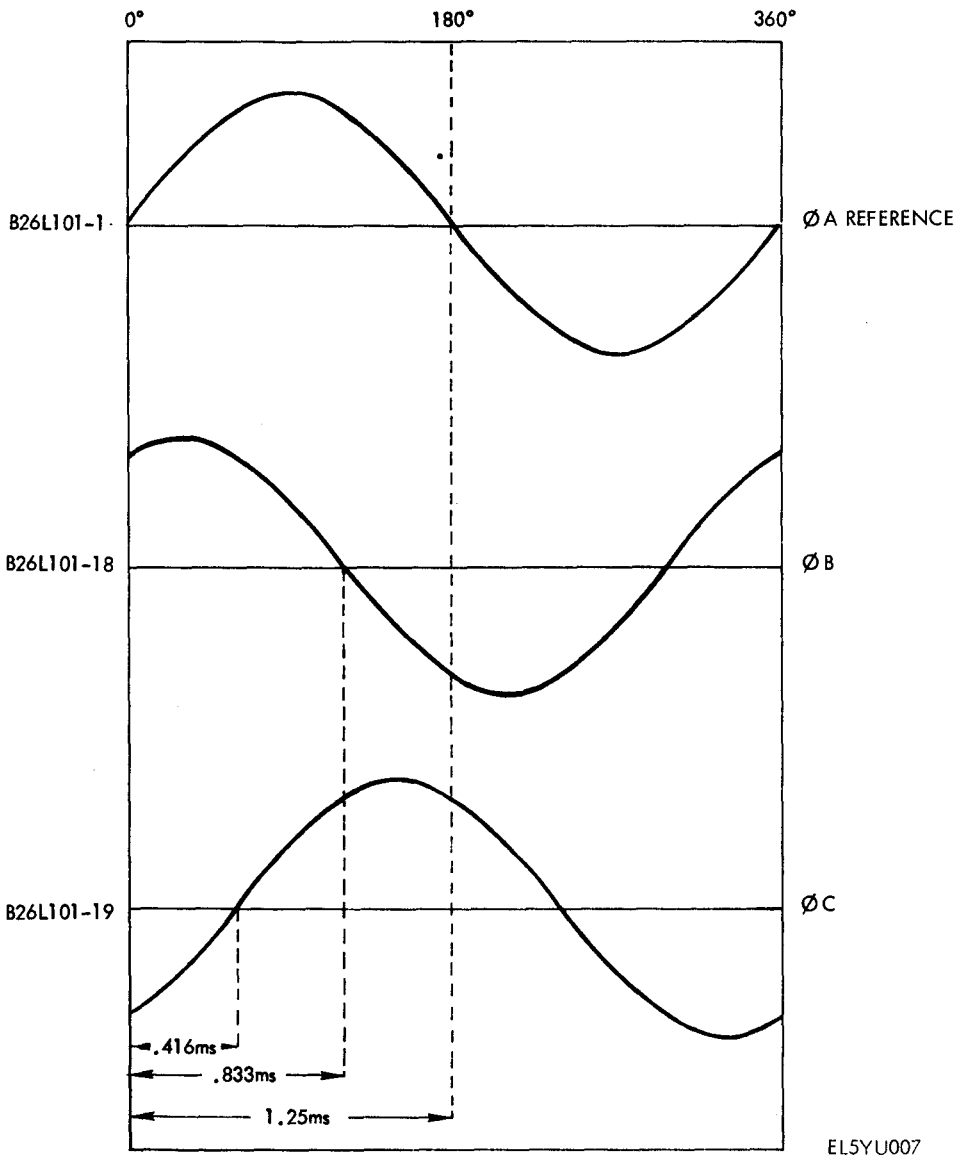


Figure 3-4. Output PhaseRelationship.

transistors B26Q110 and B26Q111, turn off power supply and set output to 0 volt, and check for open or shorted capacitor B25C108 with an ohmmeter. Redate capacitor if defective. (If capacitor is not defective, replace appropriate diode B26CR110 or 326CR111).

d. If input current was excessive, troubleshoot inverter in accordance with paragraph 3-18. Input current shall increase to 10 amperes at +15 to +16 vdc, then drop to 4-6 amperes at +28 vdc. Do not allow input current to exceed these values.

NOTE

Because of current levels in this circuit, transistors B26Q110 and B26Q111 shall be replaced as a pair.

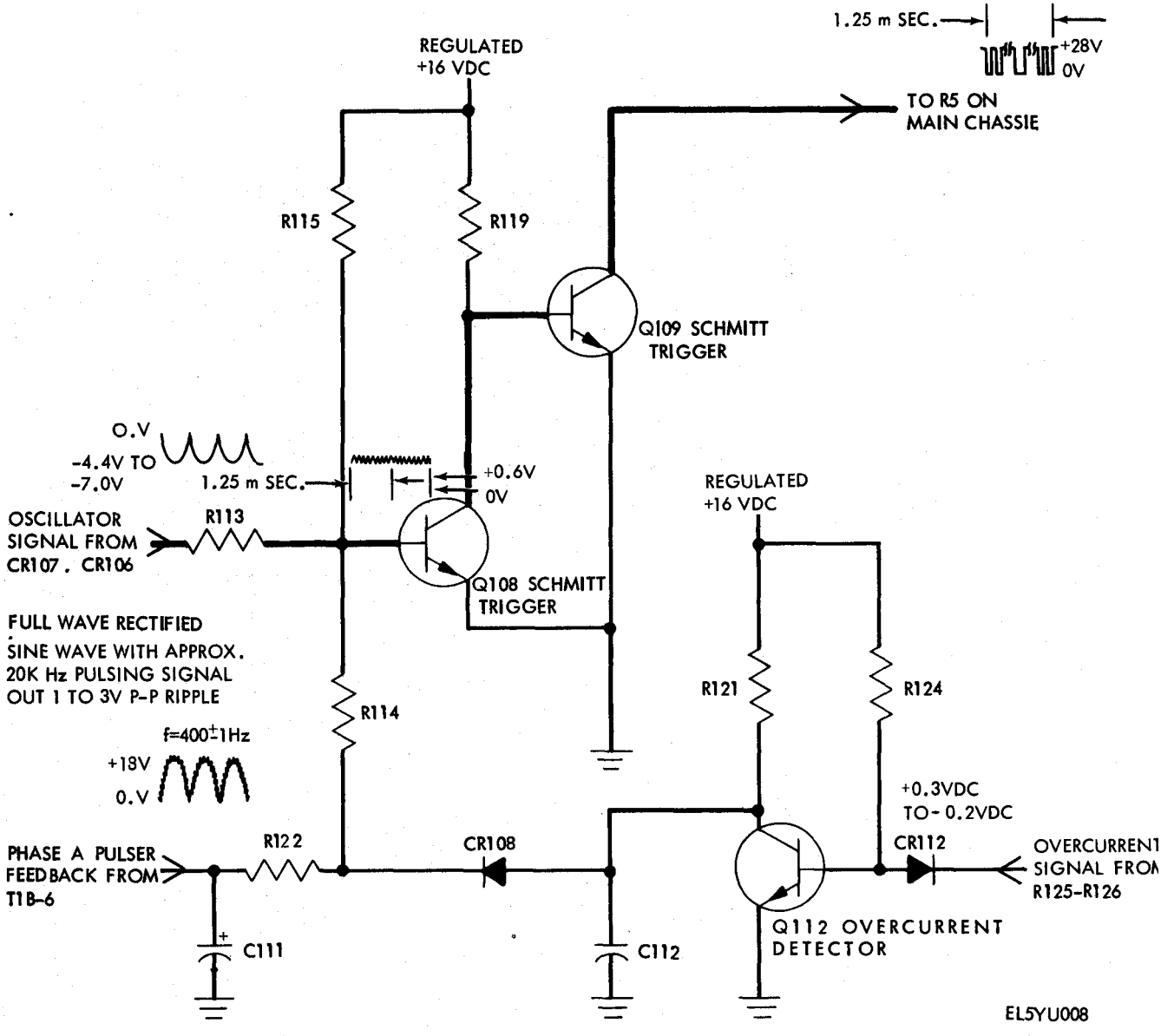


Figure 3-5. Pulser Driver Detailed Schematic Diagram.

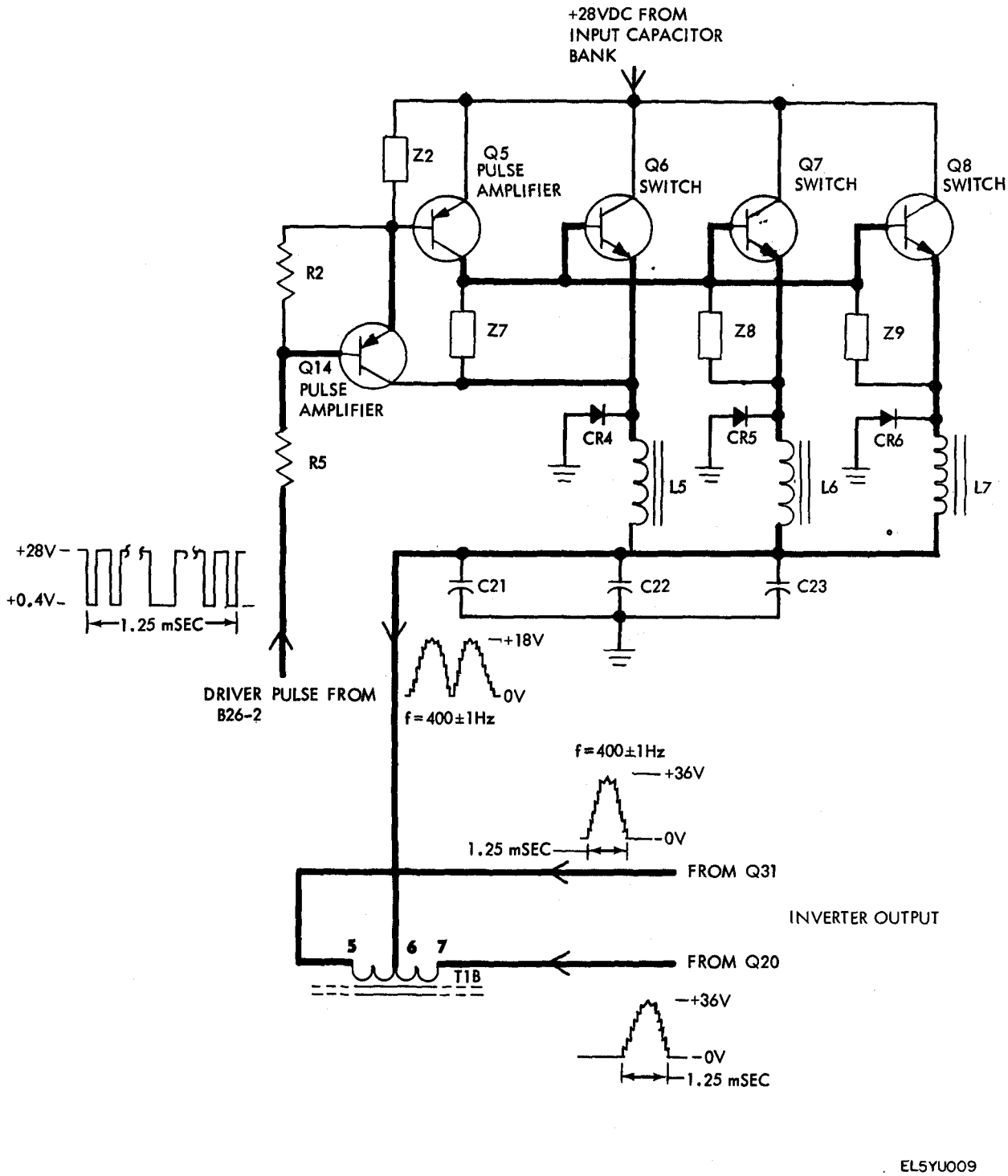


Figure 3-6. Pulser Detailed Schematic Diagram.

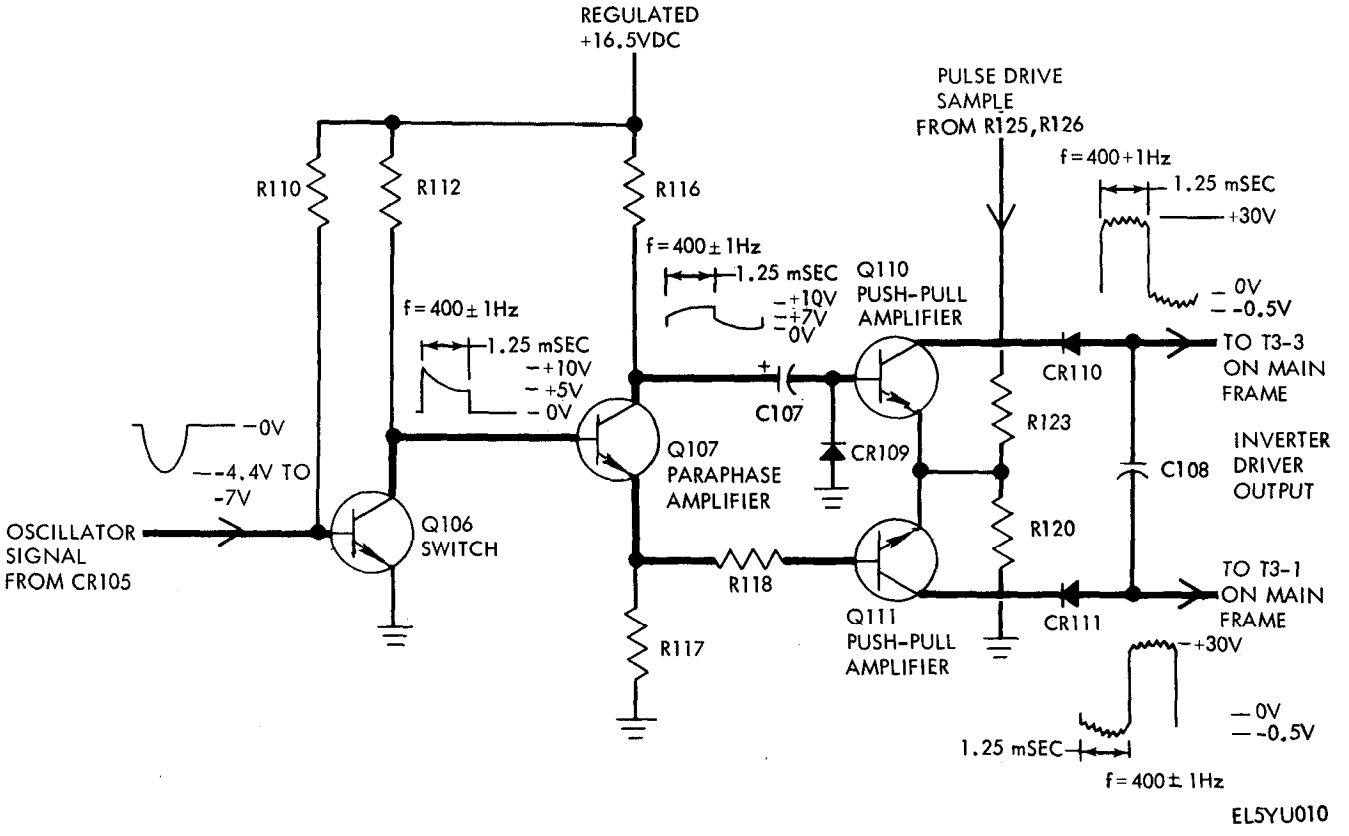


Figure 3-7. Inverter Driver Detailed Schematic Diagram.

3-18. Inverter

a. Remove leads from terminals 5 and 7 of T1B (fig. 3-8).

b. Using an ohmmeter, check for a short circuit between the lead disconnected from terminal 5 of transformer T1-5 and terminal 8 of transformer T3. If a short circuit is indicated, remove nuts and lugs from transistors A2Q29, Q30, Q31 (fig. 3-14, sheet 2) and check for open or shorted components with an ohmmeter. Replace any open or shorted components.

c. Using an ohmmeter, check for a short circuit between the lead disconnected from terminal 7 of transformer T1B and terminal 8 of transformer T3. If a short circuit is indicated, remove nuts and lugs from transistors A2Q20, Q21, Q22 (fig. 3-14, sheet 2) and check for open or shorted components with an ohmmeter. Replace any open or shorted components.

d. If no components are shorted or open, replace transformer A2T3.

e. Once all shorted or open elements have been isolated and replaced, reinstall lugs and nuts on transistors A2Q20 through A2Q22 and A2Q29 through A2Q31 (fig. 3-14, sheet 2) and reconnect leads to terminals 5 and 7 of transformer T1B. Apply +28 vdc to inverter and check voltage at B26CR110 anode and B26CR111 anode (fig. 3-7) with an oscilloscope. If voltages are not within limits, refer to paragraph 3-17 to determine cause.

3-19. Current Limit Detector and Time Delay

(fig. 3-9)

a. Check for open or shorted overcurrent delay transistor B26Q113, dc amplifier transistors B26Q115 and Q114; capacitors B26C109, C110, C114; diode B26CR113 and resistors B25R127, R128, R129, R130, R131, R132, R133, R134, R135 with an ohmmeter.

b. If no components are open or shorted, apply +28 vdc to the inverter and check voltage at anode of diode B26CR113. Replace B26CR113 if breakdown is indicated.

NOTE

It maybe necessary to perform the following checks with inverter operating into a load.

c. If input current is excessive, adjust power supply output to 0 volt. Slowly increase power supply voltage while observing input current. Input current shall increase to 10 amperes at +15 to +16 vdc, then drop to

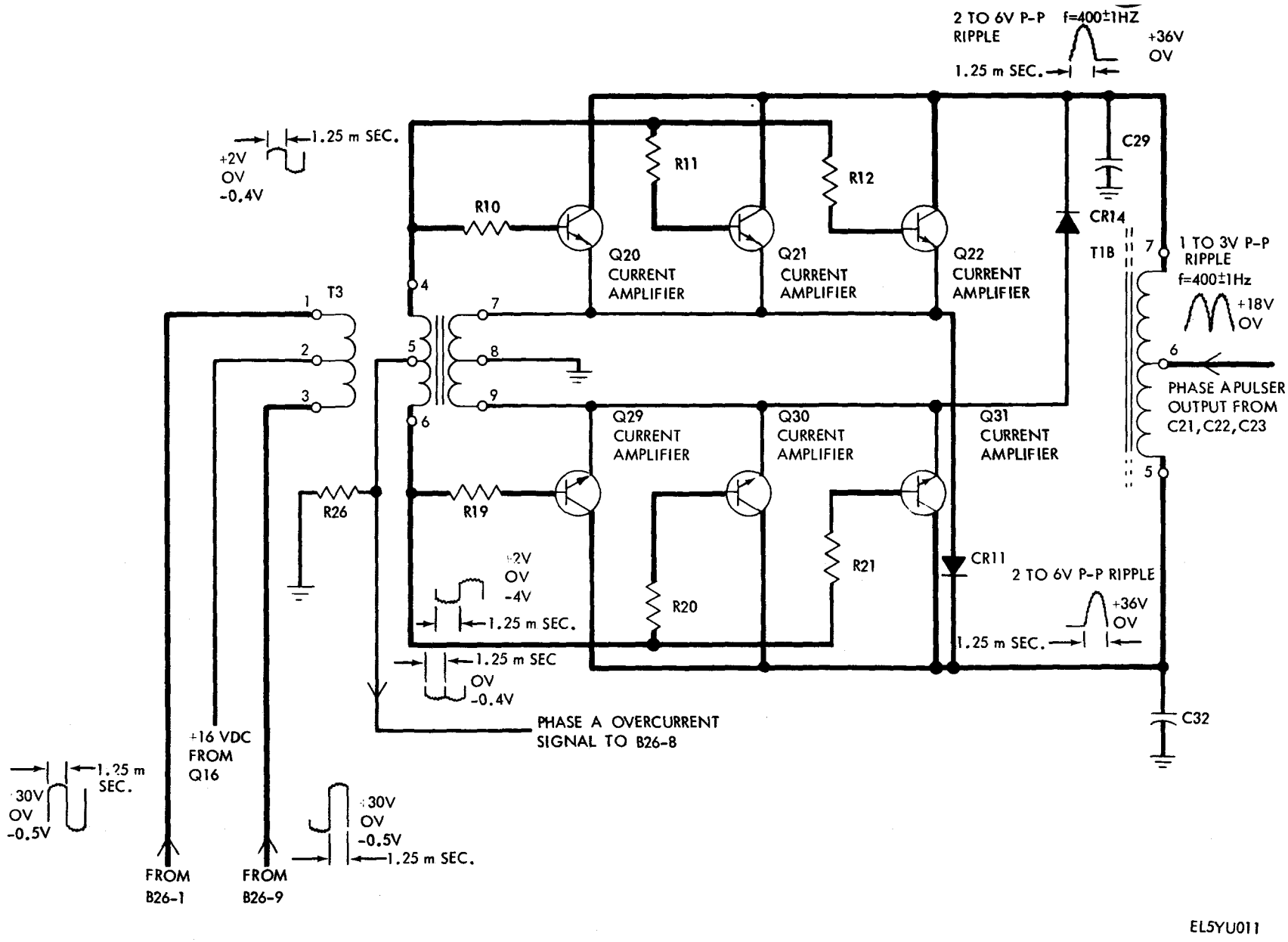


Figure 3-8. Inverter Detailed Schematic Diagram.

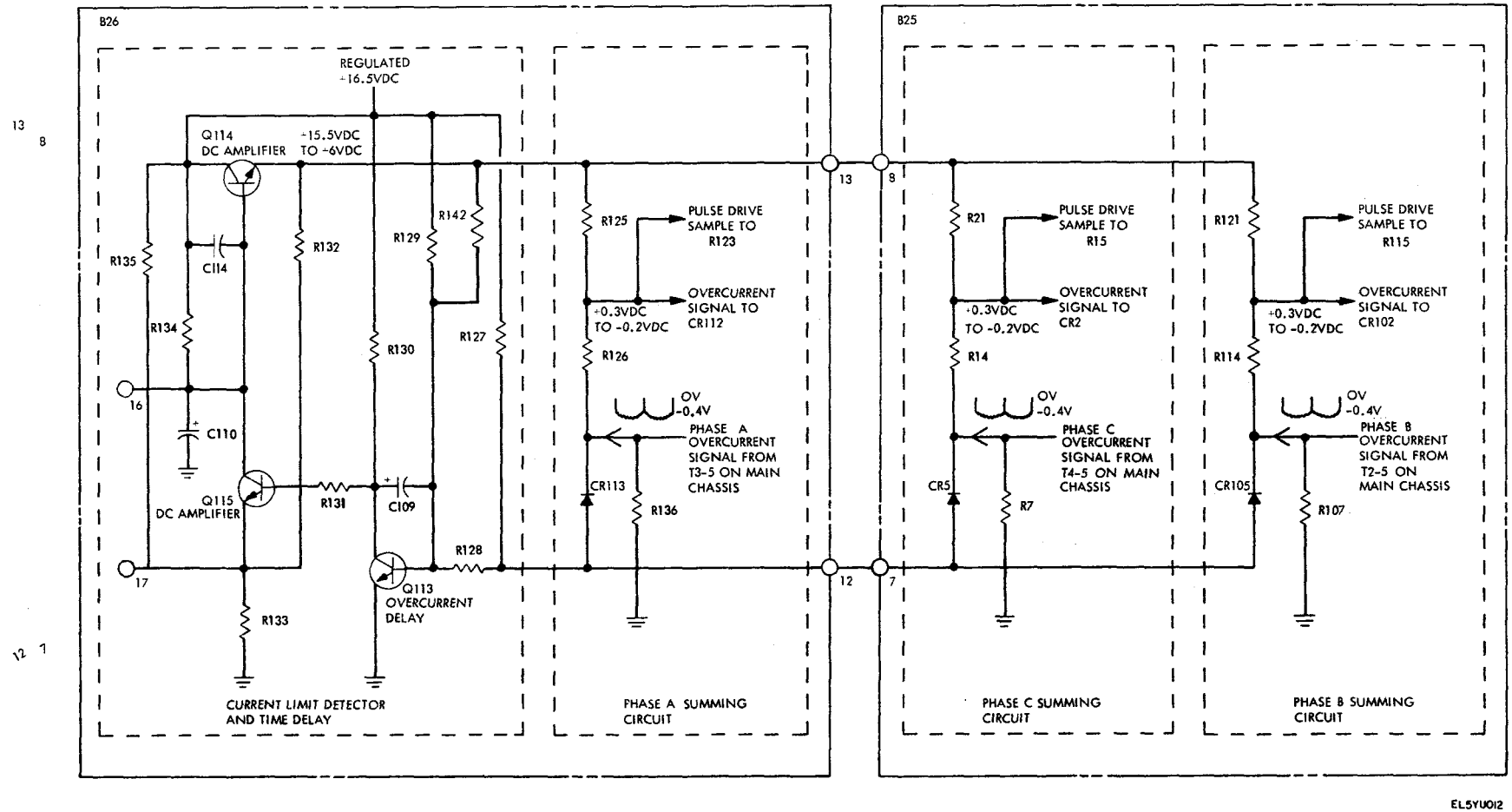


Figure 3-9. Current Limiting Detailed Schematic Diagram.

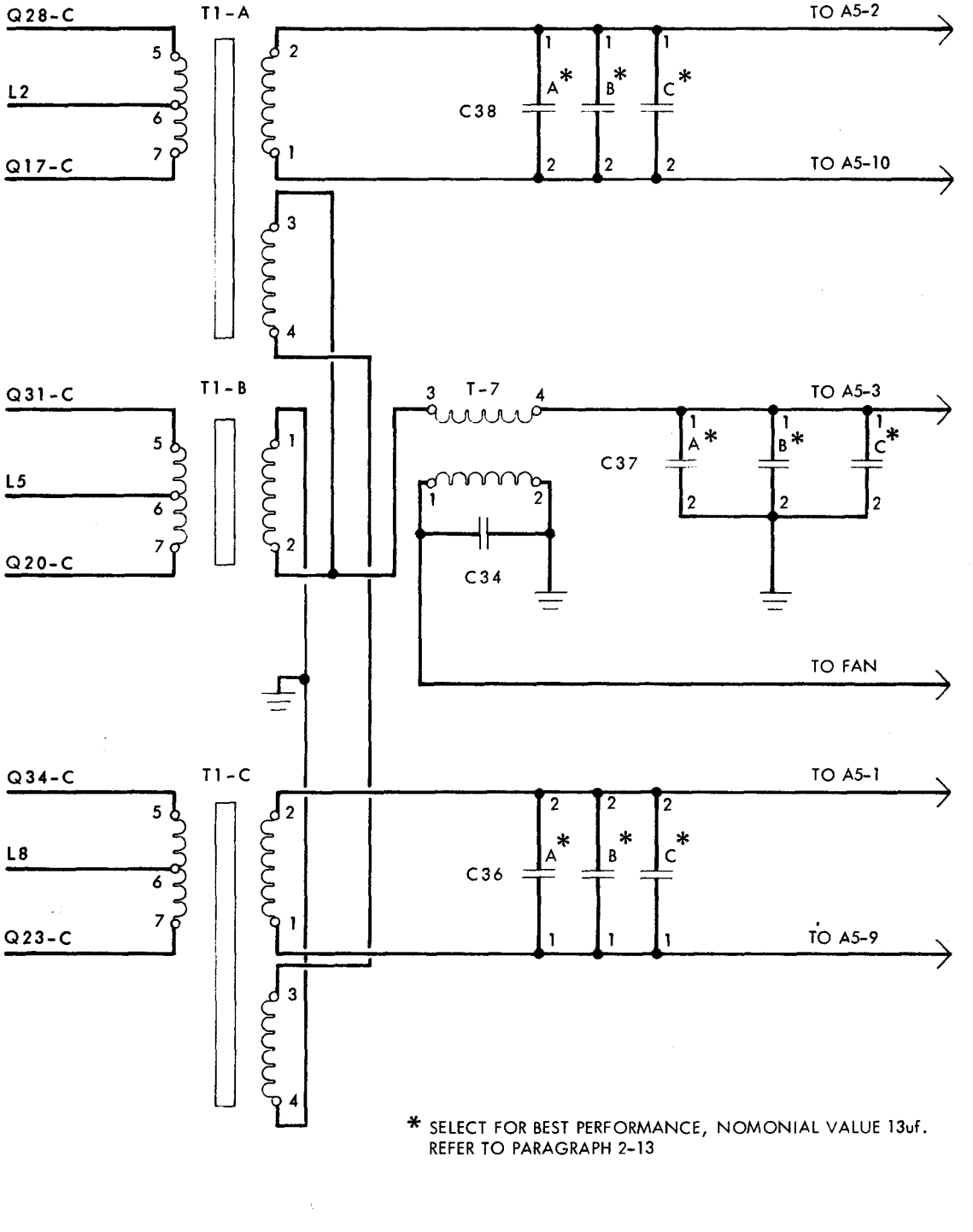


Figure 3-10. Power Transformer Detailed Schematic Diagram.

4-6 amperes at +28 vdc. Input current shall not exceed these values. If input current is excessive, troubleshoot inverter in accordance with paragraph 3-18.

d. Check chassis ground connections of T2, T3, and T4. Clean any corrosion, dirt, or oil from connections. Screws shall be torqued to 10 inch-pounds upon reinstallation.

e. Final test procedure (para 3-32) shall be used to determine proper operation of this circuit.

3-20. Summing Circuit

a. Check summing resistors, B26R125, R126, and R136 with an ohmmeter (fig. 3-9).

b. Apply +28 vdc to inverter. With an oscilloscope check waveform at the cathode of B26CR113. The waveform shall be as shown in figure 3-9. If the waveform is not correct, troubleshoot the inverter, If the waveform is correct, troubleshoot the inverter driver in accordance with paragraph 3-17.

c. Turn on power supply and slowly increase output voltage of power supply while observing input current. During normal operation, input current shall increase to 10 to 12 amperes at +15 to +16 vdc, then drop to 4-6 amperes at +28 vdc. If input current is excessive, troubleshoot inverter in accordance with paragraph 3-18.

3-21. Power Transformer

a. Check for open or shorted capacitors C36, C37 or C38.

b. Disconnect wires from pins 1 through 7 of power transformer T1B. Connect ohmmeter between pins 2 and 7. The meter shall read open. If the reading is open, measure the resistance between 1 and 2 and 5 and 7. The resistance shall be less than 5 ohms.

c. If all resistance readings are correct, measure each pin of the transformer to ground. The ohmmeter shall read open. If any of the pins read 0-ohms replace transformer.

d. If transformer is not open or shorted, replace all wires and check waveforms at pins 1 and 2. If waveforms are not correct (fig. FO-1), check waveforms at

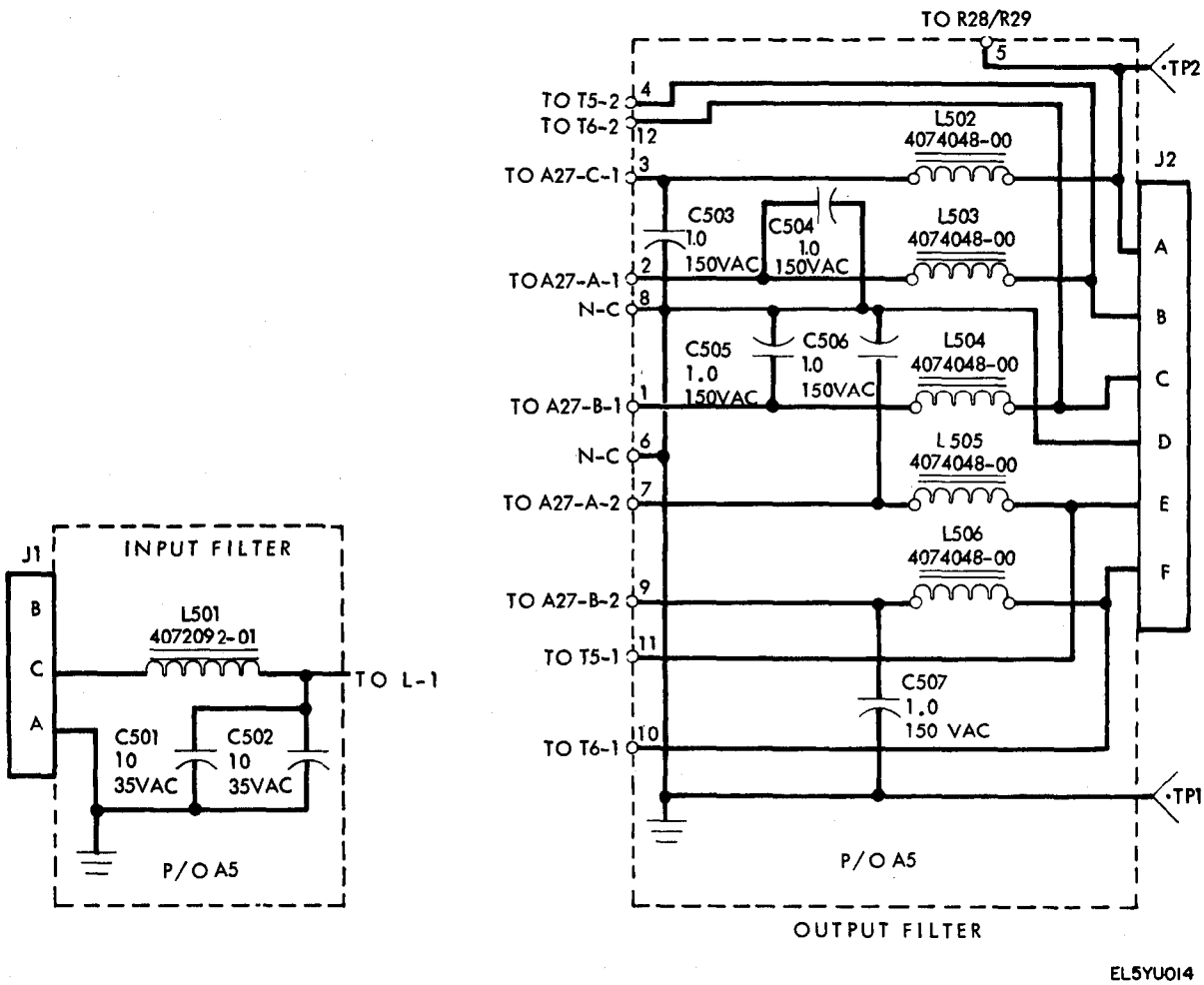


Figure 3-11 Input/Output Filter Detailed Schematic Diagram.

pins 5, 6, and 7. If waveforms are correct, replace transformer. If waveform on pin 6 is not correct, troubleshoot pulser as described in paragraph 3-16. If waveform on pin 5 or 7 is not correct, troubleshoot inverter as described in paragraph 3-18.

3-22. Output Filter

a. The output filter is an encapsulated nonrepairable module and is part of the input filter module. If distortion is excessivein output voltage, replace filter module after preceding analysis has been considered.

b. Perform output distortion checks and adjustments in accordance with paragraph 3-27.

NOTE

An open capacitor in this filter may cause high input current when the unit is operating in the Delta mode but not in the WYE mode. Always check operation in both modes.

3-23. Adjustments

Table 3-8 lists the adjustments and circuit involved which affect the operation of the inverter. The paragraphs following the table give the method for making these adjustments. Any deviation from the procedure as listed will cause improper operation of the inverter.

Table 3-8. Adjustments and Alignments

Inverter adjustment	Circuit involved	Adjustment procedure
Output frequency adjustment	oscillator circuit	Paragraph 3-24
Output voltage adjustment	Regulator circuit	Paragraph 3-25
Output distortion	Pulser output circuit	Paragraph 3-27
Short circuit time delay	Current limiting circuit	Paragraph 3-26

3-24. Oscillator Frequency Adjustment

a. To adjust the output frequency proceed as follows:

(1) If the inverter has not been previously opened, do so as described in paragraph 3-28. Disassemble until printed circuit boards are accessible.

(2) Disconnect the +28 vdc bus at input capacitor bank.

(3) Disconnect the following wires at the PCB.

B26E18	WHT/GRA
B26E19	WHT/BLK
B25E20	BRN/BLK

(4) Connect frequency counter to B26L101 pin 1.

(5) Apply 28 vdc to the inverter.

NOTE

Input current will not exceed 1.0 ampere. If current is high, troubleshoot inverter as de scribed in paragraph 3-8.

(6) Check frequency on frequency counter; it shall e 400 ±0.5 Hz. If the frequency is not 400 ±0.5 Hz, roceed to (7) below.

(7) If the oscillator frequency is high, increase the value of C104. If the frequency is low, decrease the value of C104.

NOTE

A 0.01 µfd change in capacitance will change the frequency approximately 5 Hz.

(8) Connect frequency counter to B25L1 pin 2.

(9) Check frequency on frequency counter; it shall be 400 ±0.5 Hz. If the frequency is not 400 ±0.5 Hz, refer to (7) above.

NOTE

Refer to table 3-1 for correct capacitor reference designation for phases B and C.

(10) Connect frequency counter to B25L101 pin 1.

(11) Check frequency on frequency counter; it shall be 400 ±0.5 Hz. If the frequency is 400 ±0.5 Hz, proceed to (12) below. If the frequency is not 400 ±0.5 Hz, refer to (7) above.

(12) Recheck frequency at B26L101 pin 1, B25L1 pin 2 and B25L101 pin 1 to ensure proper frequency before proceeding.

(13) Turn off the 28 vdc power to the inverter.

(14) Replace the wires removed in (2) and (3) above.

NOTE

Apply HYSOL #22 to all solder connections made during this adjustment procedure.

b. If no other troubleshooting or adjustment is indicated, reassemble unit as described in paragraph 3-29 and check inverter for proper operation as described in Section V, Final Tests.

3-25. Output Voltage Adjustment

a. To adjust the Phase A output voltage, proceed as follows:

(1) Connect inverter to test fixture as shown in figure 3-18.

CAUTION

Isolate voltmeter chassis from earth ground to avoid damage to inverter.

(2) Set test fixture switches as follows: S1–No load; S2–WYE; S3–phase A; S4–+1.0; S5-Off.

(3) Energize the test equipment and slowly (over approximately 10 seconds) raise the input voltage to +28 vdc. If input current exceeds approximately 10

amperes at any point, turn off the equipment and troubleshoot as described in paragraph 3-8.

NOTE

Input current should reach approximately 10 amperes when the input voltage reaches + 15 to +16 vdc. Input current should then drop to a final value of approximately 4 to 6 amperes at +28 vdc.

(4) With input set at +28 vdc, the output indication on the true RMS voltmeter shall be exactly 115.5 vac. If it is not, adjust potentiometer B26R109 for 115.5 vac on the voltmeter.

NOTE

Brush on protective coating to reseal potentiometer adjustment screws after this adjustment procedure has been completed.

(5) If the output cannot be set to 115.5 vat, turn off the equipment and troubleshoot inverter.

b. Phase B Output Voltage.

(1) Set test fixture switches as follows: S1–No load S2–WYE; S3–phase B; S4–+10; S5–Off.

(2) Repeat steps 3 to 5 of phase A adjustment procedure, except if adjustment is necessary to adjust B25R1.

c. Phase C Output Voltage.

(1) Set test fixture switches as follows: S1–No load; S2–WYE; S3–Phase C; S4–+1.0; S5–Off.

(2) Repeat steps 3 to 5 of phase A adjustment procedure, except if adjustment is necessary to adjust B25R101.

3-26. Adjustment of Overcurrent Shutdown Time

a. Use test procedure 3-33 to check for proper times.

b. If T foldback is less than 5 seconds, decrease B26R142. If T foldback is too slow, increase B26R142. (See figure FO-3).

c. If unit fails to recover properly after removal of the short, it may be necessary to decrease B26R142 further.

d. The range of R142 is from 240K ohms to 560K ohms.

3-27. Output Distortion Adjustment

a. To adjust the output distortion, proceed as follows:

NOTE

If the inverter fails to meet any voltage, current, frequency or phasing requirement during the course of the following test, troubleshoot the defective circuits in accordance with the applicable paragraph. After repairs have been made, repeat the entire output distortion check.

(1) The output distortion check shall be performed

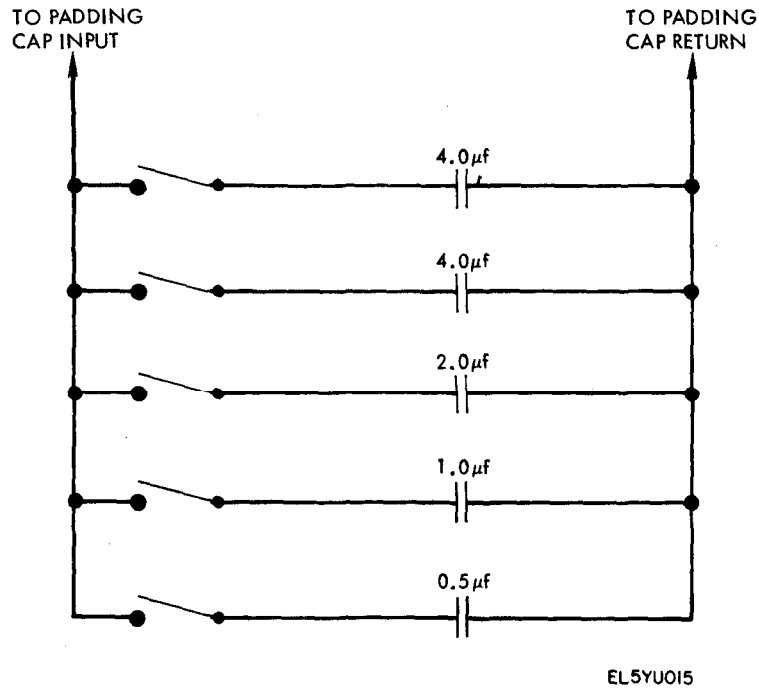


Figure 3-12. Output Padding Schematic Diagram.

with the inverter completely assembled to provide adequate cooling air. Note that if the output distortion check does not meet specifications, the unit will have to be disassembled to adjust the affected circuits.

(2) Connect the inverter to the test equipment as shown in figure FO-6.

CAUTION

Isolate the true RMS voltmeter, the distortion analyzer and the frequency counter chassis from earth ground to avoid inadvertent shorts in the inverter output.

(3) If distortion exceeds that specified in table 3-9, select a new capacitance value which gives best overall distortion while not exceeding specified limits. The capacitors to be padded or replaced are A27C37, for phase A, A27C36 for phase B, and A27C38 for phase C.

(4) Decrease the value of the tuning capacitor is the no load distortion is excessive. Increase the value of the tuning capacitor if the full load distortion, especially for the +0.75 power factor (inductive load) condition, is excessive.

(5) After the tuning capacitor value has been modified, repeat the no load test above, the full load inductive test above and the procedure or procedures which originally failed.

(6) If the output distortion still does not meet specifications, further modify the tuning capacitor as described in the procedures above. If the output distortion is found to be within specifications for these worse case conditions, repeat the entire distortion test to be sure that the output distortion has not been increased in other test conditions.

b. When the output distortion meets the specified levels, turn off the test equipment. If no further troubleshooting or adjustment procedures are necessary, disconnect the test equipment and reassemble the inverter.

3-28. Disassembly Instructions

a. To disassemble the basic assembly, proceed as follows:

(1) Remove 18 No. 4-40x¼ screws (10, fig. 3-13) from rear cover (9).

(2) Remove rear cover.

(3) Remove 18 No. 4-40x¼ screws (10) and seven No. 4-40x½ panhead screws from front cover (17).

CAUTION

Wires are connected to front cover via input/output filter (20) and fan (13). Do not force cover as damage to wire or connections may result.

(4) Remove 6 No. 4-40x¼ screws (8) from top of nverter.

(5) Remove 6 No. 4-40x % screws (10) from bottom of inverter.

(6) Separate pulser assembly (2) from inverter assembly (12).

(7) Disconnect filter cable by removing a hexhead screw (3), flatwasher (5), lockwasher (6), and nut(7).

(8) Remove front cover.

CAUTION

Wires are connected from the pulser assembly to the inverter assembly. Caution must be taken not to break them when separating the units.

b. To disassemble front cover assembly (17, fig. 3-13), proceed as follows:

(1) Remove 4 No. 4-40 x 3/16 screws (15) and 4 clamps (16) from front cover assembly.

(2) Remove fan (13) from front cover assembly.

(3) Mark and disconnect wires attached to fan.

(4) Remove 8 No. 4-40x3/8 screws (18) from front cover assembly.

(5) Remove input/output filter (20) from front assembly.

(6) Mark and disconnect wires attached to **in**put/output filter.

c. To disassemble pulser assembly Al (fig. 3-14, sheets 1 and 2) proceed as follows:

(1) Mark and disconnect wires to coils L2-L10 (4, fig. 3-14, sheet 1).

(2) Remove No. 4-40 x ¼ x ¼ screws (30, fig. 3-14, sheet 2) from pulser chassis.

(3) Mark (schematic reference designation) and remove coils L2-L10.

(4) Mark and disconnect (red) wires from capacitor assembly A12 (13) to pulsar assembly.

(5) Remove 16 No. 4-40x3/16 screws (20) from pulser chassis.

(6) Remove capacitor assembly. To disassemble capacitor assembly, proceed as follows:

(a) Mark and disconnect (red) wires on capacitors Cl through C17 (4, fig. 3-15).

(b) Remove 18 No. 4-40 x3/16 screws (7) from plate (6).

(c) Remove side plate.

(d) Remove insulator assemblies (3 and 5).

(7) Remove plate (6, fig. 3-15) from pulser chassis.

NOTE

The following portion of this procedure is to disassemble transistors Q13-Q15 (7, fig. 3-14). Instructions will be given to disassembly one transistor. If more than one transistor is to be removed, repeat this procedure for each transistor.

(8) Mark and disconnect wires that attach to the base and emitter of transistor.

(9) Note location and remove resistors (8 and 9) from emitter, collector, and base of transistor.

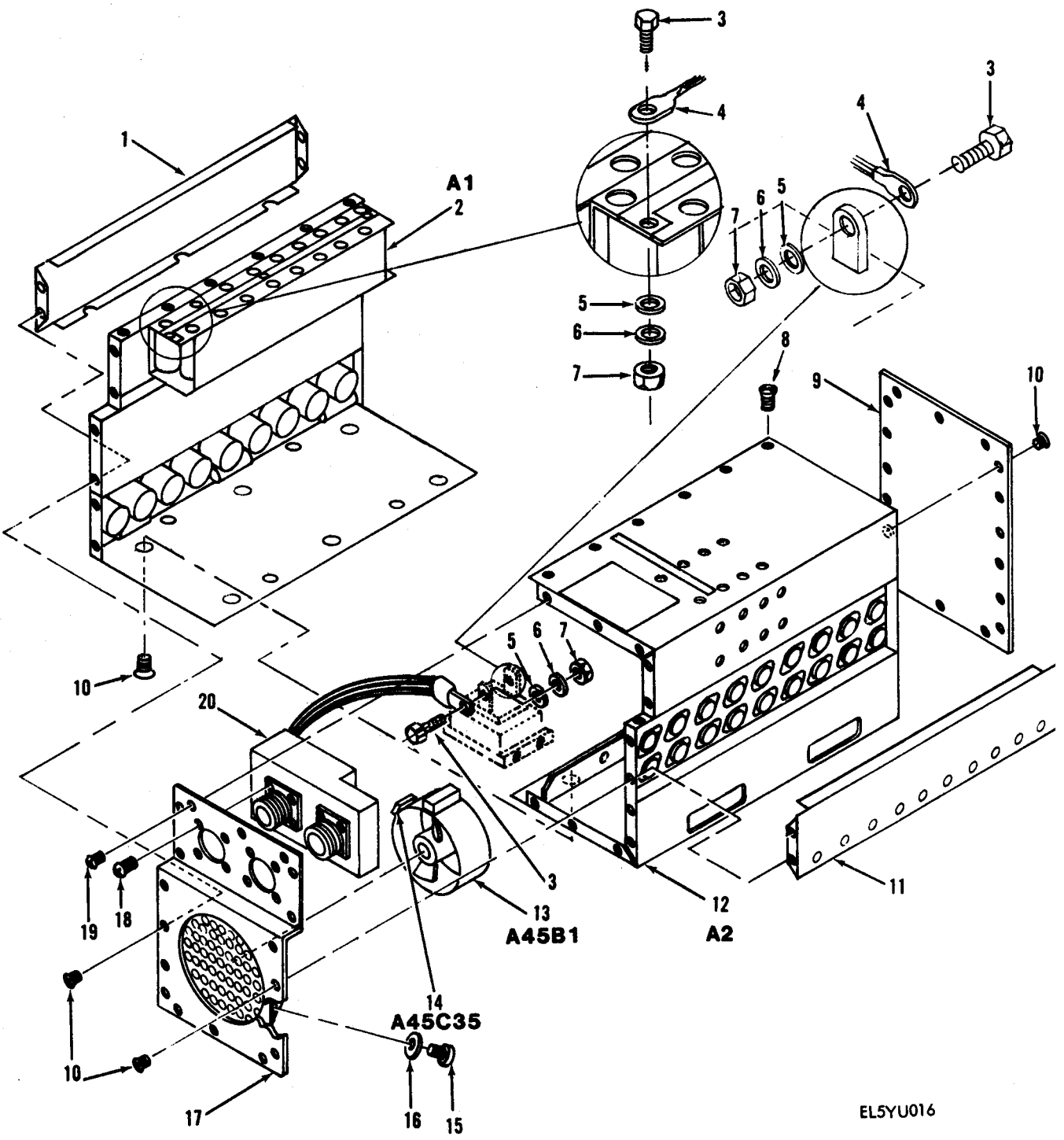
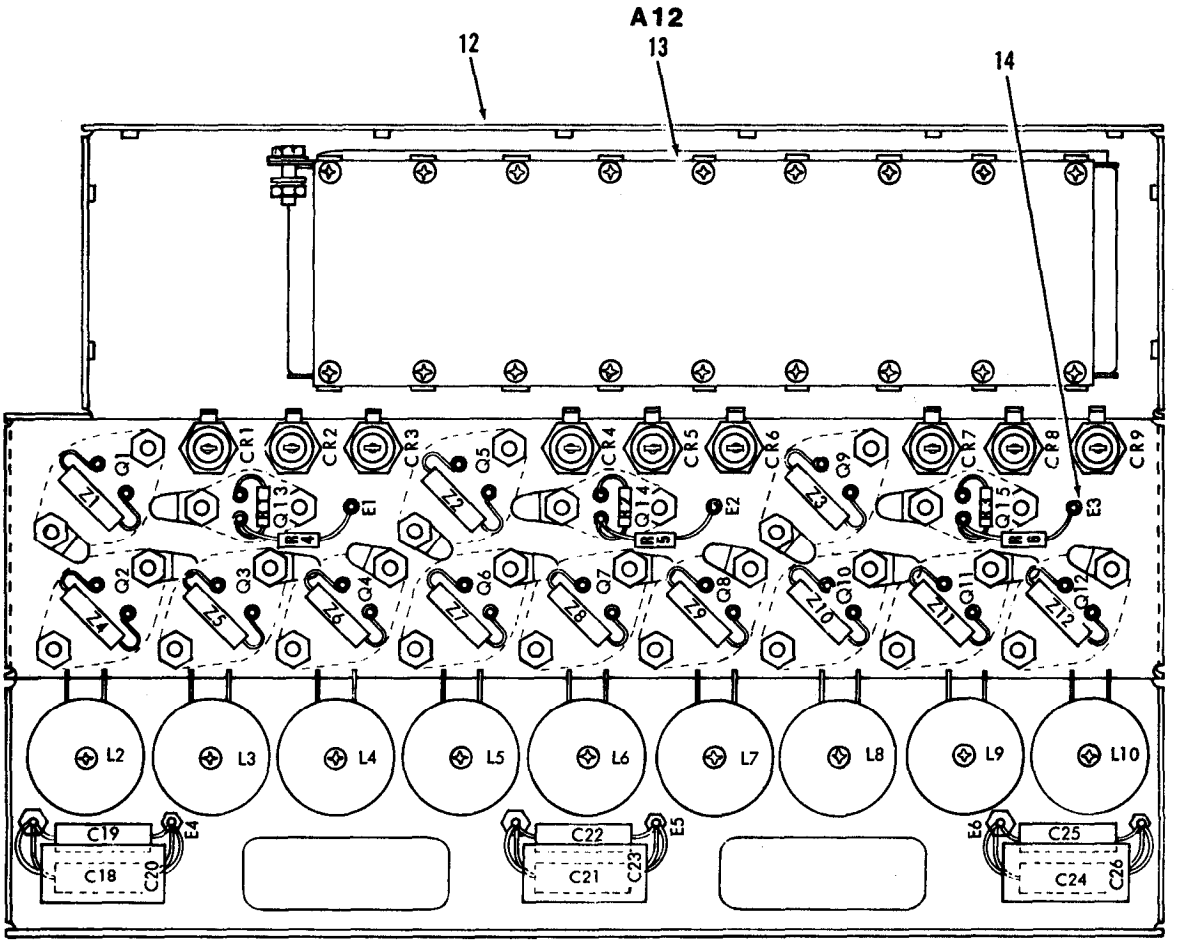


Figure 3-13. Inverter Power Supply.



LEGEND

REF DES	ITEM NO.	REF DES	ITEM NO.	REF DES	ITEM NO.	REF DES	ITEM NO.
C18	1	CR7	3	Q4	6	R4	9
C19	1	CR8	3	Q5	5	R5	9
C20	2	CR9	3	Q6	6	R6	9
C21	1	L2	4	Q7	6	Z1	10
C22	1	L3	4	Q8	6	Z2	10
C23	2	L4	4	Q9	5	Z3	10
C24	1	L5	4	Q10	6	Z4	11
C25	1	L6	4	Q11	6	Z5	11
C26	2	L7	4	Q12	6	Z6	11
CR1	3	L8	4	Q13	7	Z7	11
CR2	3	L9	4	Q14	7	Z8	11
CR3	3	L10	4	Q15	7	Z9	11
CR4	3	Q1	5	R1	8	Z10	11
CR5	3	Q2	6	R2	8	Z11	11
CR6	3	Q3	6	R3	8	Z12	11

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NOTE: PREFIX ALL REFERENCE DESIGNATORS WITH A1

Figure 3-14 ①. Pulser Assembly A1 (Sheet 1 of 2).

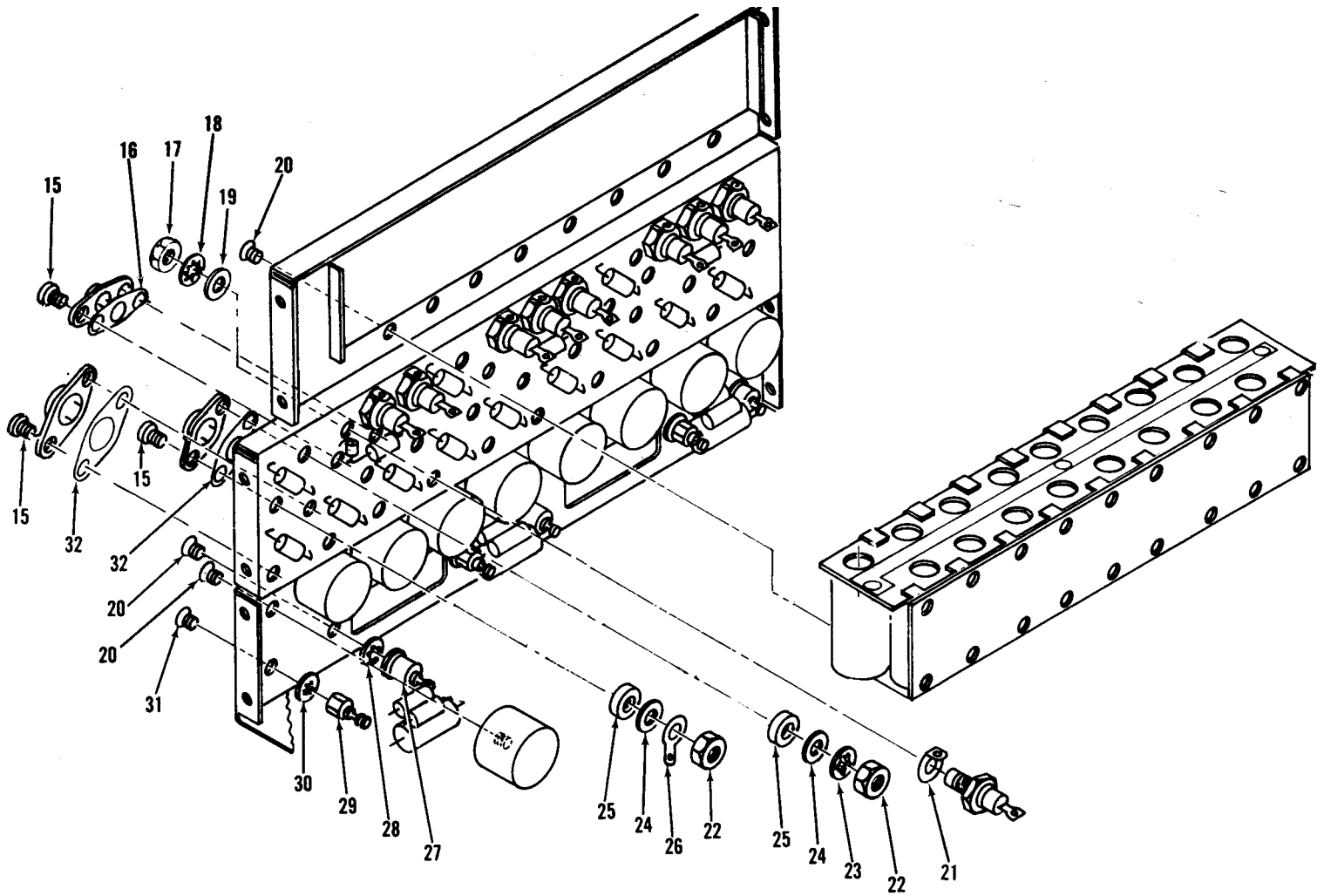


Figure 3-14 ②. Pulser Assembly A1 (Sheet 2 of 2).

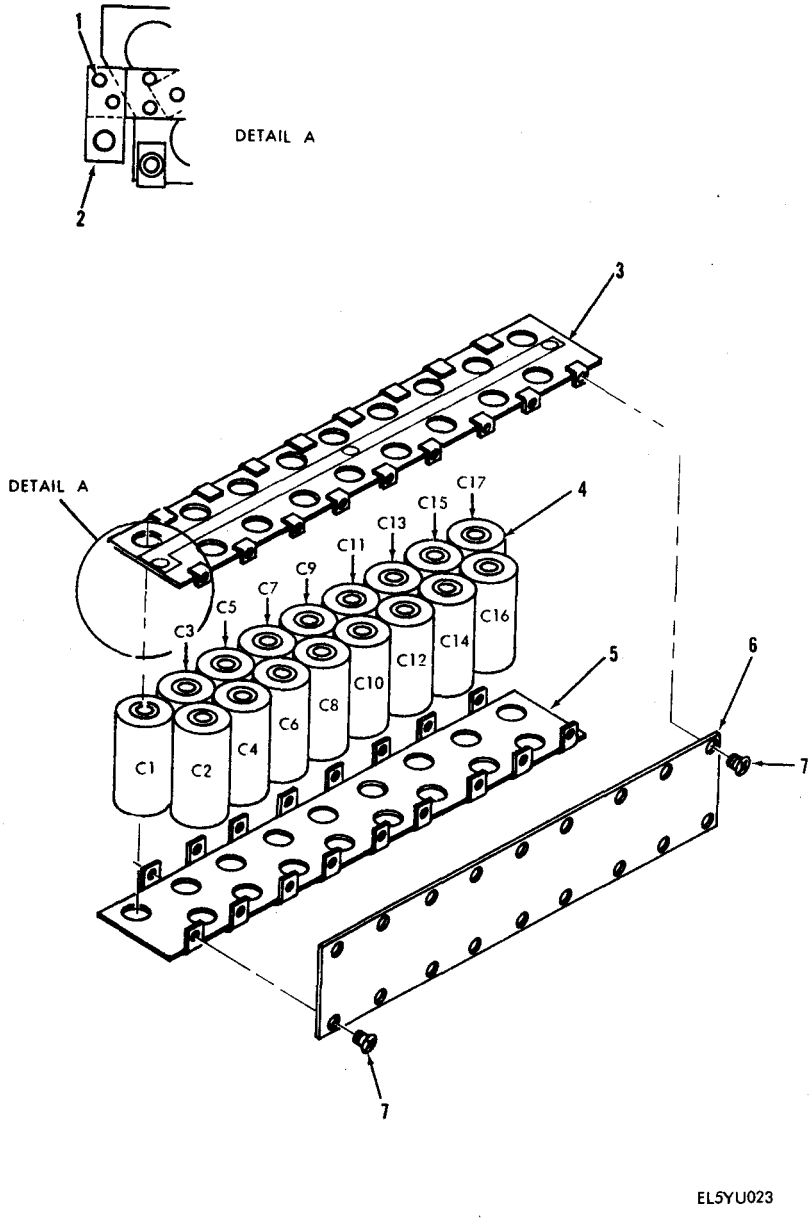


Figure 3-15. Capacitor Assembly A12.

(10) Remove 1 No. 6-32 x ½ screws (15) from transistor. Note order of removal of nut (22, fig. 3-14, sheet 2), spade lug (26), flat washer (24), and insulated washer (25) from screw (15).

(11) Remove transistor from chassis.

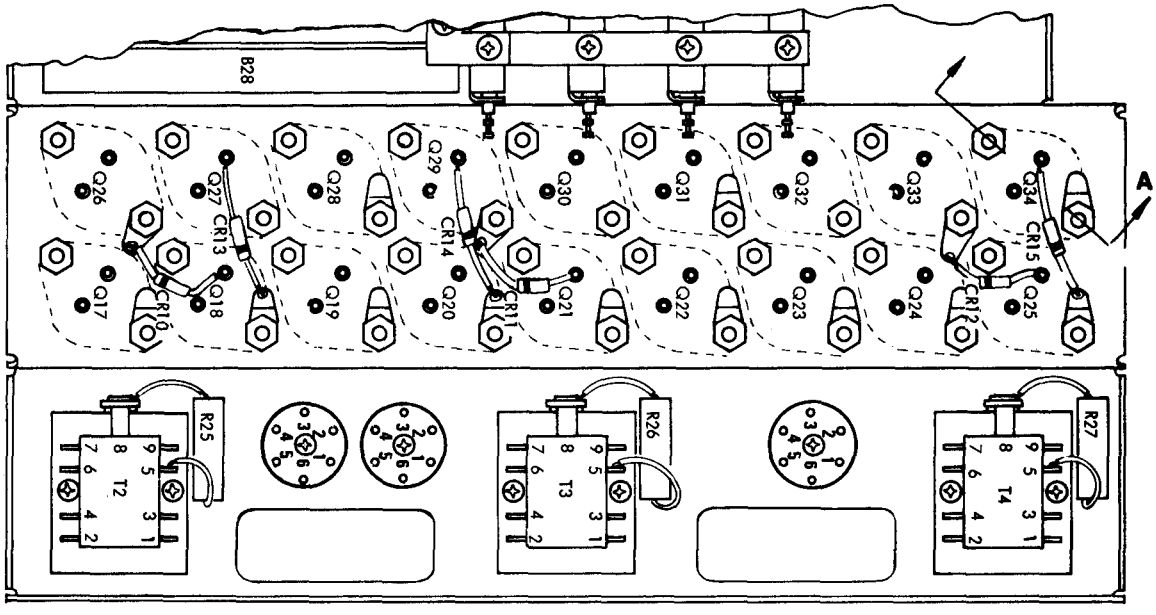
(12) Remove transistor insulator (31) from transistor.

CAUTION

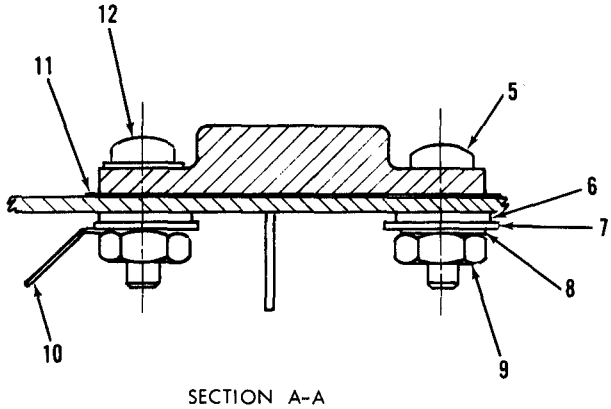
When assembly of transistors is to be performed, extreme caution shall be taken when assembling insulating material (25 and 31) and mounting hardware. Any assembly other than what is indicated by this procedure will cause serious damage to the transistor and associated circuitry.

NOTE

The following portion of this procedure is to disassemble transistors Q1-Q14 (5 or 6, fig. 3-14), Instructions will be given for the disassembly of one transistor. If more than one transistor is to be removed, repeat (13) through (17) below for each transistor.



NOTE: TRANSFORMER SECTION REMOVED FOR CLARITY. SEE SHEET 2 FOR COMPLETE ASSEMBLY DETAILS.



SECTION A-A
12 PLACES

LEGEND

REF DES	ITEM NO	REF DES	ITEM NO
CR10	1	Q26	2
CR11	1	Q27	2
CR12	1	Q28	2
CR13	1	Q29	2
CR14	1	Q30	2
CR15	1	Q31	2
Q17	2	Q32	2
Q18	2	Q33	2
Q19	2	Q34	2
Q20	2	R25	3
Q21	2	R26	3
Q22	2	R27	3
Q23	2	T2	4
Q24	2	T3	4
Q25	2	T4	4

NOTE: PREFIX ALL REFERENCE DESIGNATORS WITH A2.

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Figure 3-16 ①. Inverter Assemhly A2 (sheet 1 of 2).

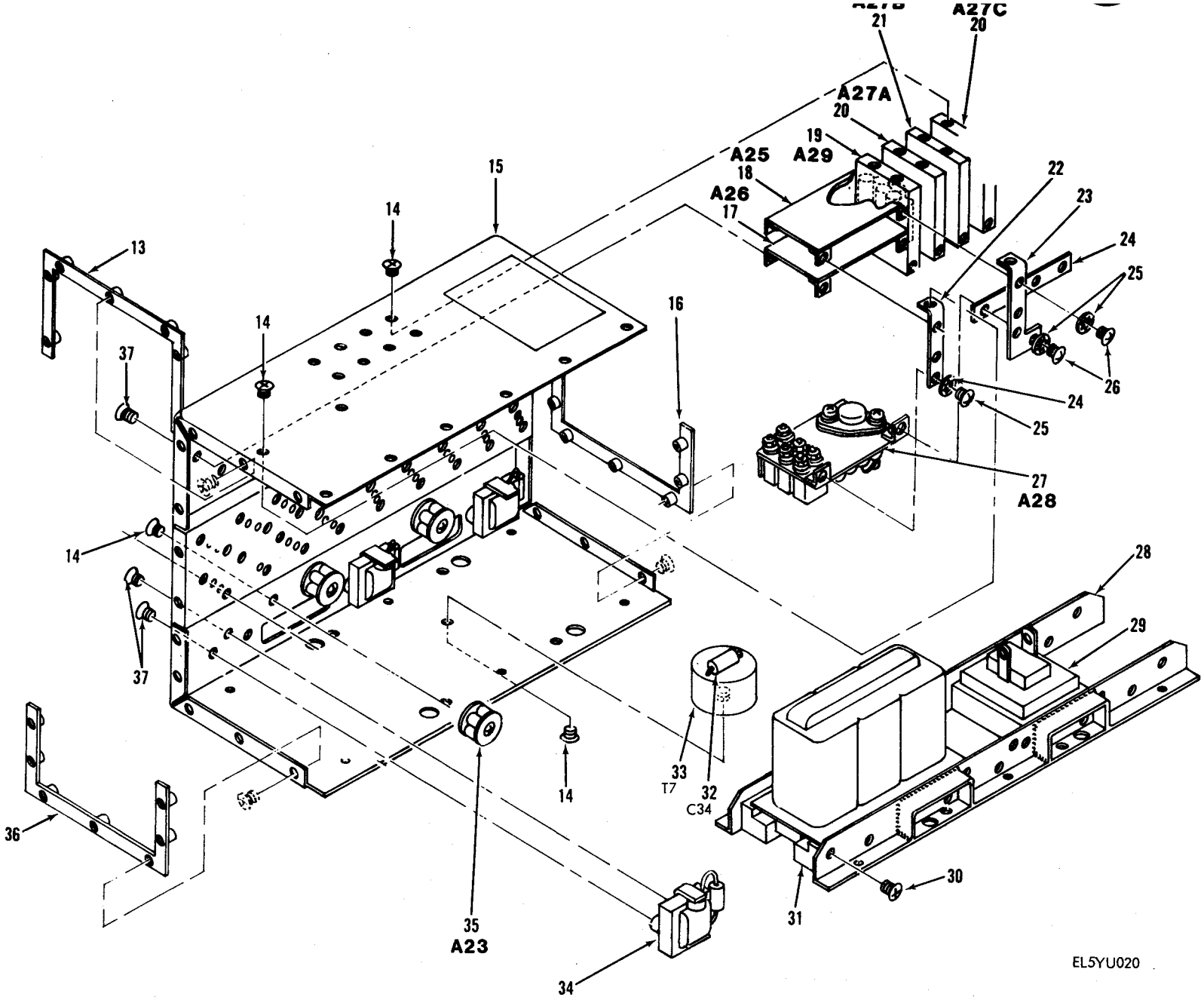


Figure 3-16 ②. Inverter Assembly A2 (sheet 2 of 2).

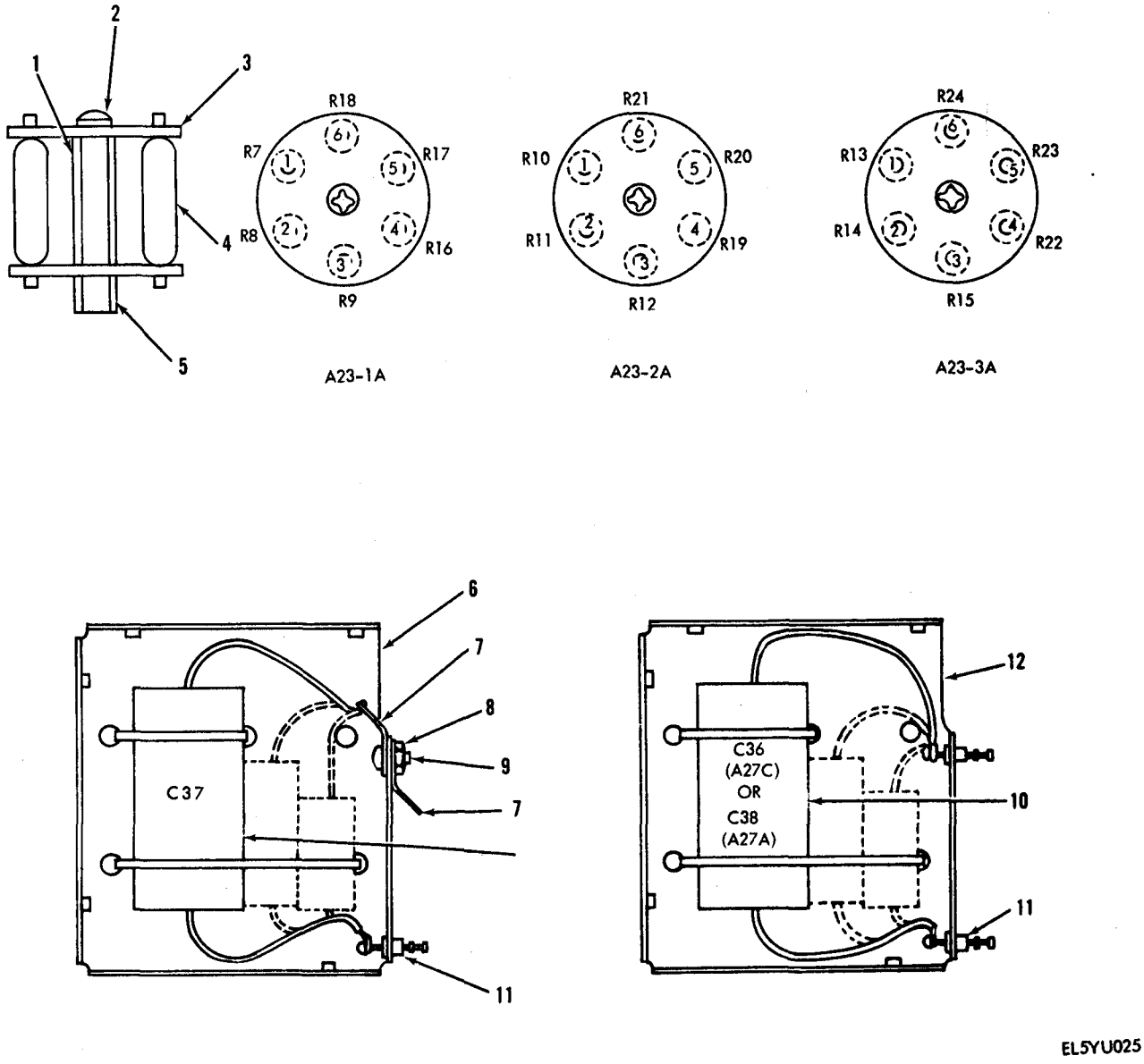


Figure 3-17. Resistor Assembly A23, Capacitor Assembly A27B, and Capacitor Assembly A27A or A27C.

(13) Mark and disconnect wires that attach to the base and emitter.

(14) Note location and remove impedance elements (10 or 11) from emitter and base of transistor.

(15) Remove two No, 6-32 x ½ screws (15) from the transistor. Note order of removal of nut (22, fig. 3-14, sheet 2), lockwasher (23), flat washer (24), and insulated washer (25) from screw (15).

(16) Remove transistor from chassis.

(17) Remove transistor insulator (31) from transistor.

CAUTION

When assembly of transistors is performed, extreme caution shall be taken when assembling insulating material (25 and 31) and mounting hardware. Any assembly other than what is indicated by the procedure and figure will cause serious damage to the transistor and associated circuitry.

(18) Note location and remove capacitors C18 through C26 (1 and 2, fig. 3-14, sheet 1) from terminals (27 and 29, fig. 3-14, sheet 2).

(19) Mark and disconnect wires attached to terminals.

(20) Remove 6 No. 4-40 x ¼ screws (30) from pulser chassis.

(21) Remove terminals (27 and 29) and washers (28) from pulser chassis.

d. To disassemble inverter assembly (fig. 3-16, sheets 1 and 2), proceed as follows:

(1) Mark and disconnect wires from transformer T7 (3) and capacitor C34 (32, fig. 3-16, sheet 2).

(2) Remove screw (14) attaching transformer to inverter assembly (15).

(3) Remove transformer and capacitor from inverter assembly.

(4) Mark and disconnect wires from T1 power transformer (31) and RF choke L1 (29).

(5) Remove power transformer assembly.

(6) Remove screws (30) from transformer brackets (28).

(7) Remove transformer mounting brackets from T1 power transformer and RF choke.

(8) Remove two screws (14) from top of inverter chassis.

(9) Remove 10 screws (26) from brackets (22, 23).

(10) Remove brackets.

NOTE

The following procedure defines the removal of capacitor modules A27 or A29 (19, 20 and 21). This procedure will define the removal of one module. If more than one module is to be removed, repeat this procedure for each capacitor module to be removed.

(11) Remove four screws (14) from top and side of inverter chassis.

(12) Remove capacitor assembly.

(13) Mark and disconnect wires attached to capacitor assembly.

(14) Remove board assemblies A25 and A26 (17, 18).

(15) Mark and disconnect wires connected to board assembly.

NOTE

To disassemble resistor assemblies A23-1, A23-2, A23-3 (35), proceed as follows. Instructions are given for the removal of one assembly. If more than one assembly is to be removed, repeat procedure for each assembly that is to be removed.

(16) Mark and disconnect six wires attached to resistor assembly.

(17) Remove screw (14) from side of inverter chassis.

(18) Remove resistor assembly.

(19) Note location and disconnect jumper wires from rear of resistor assembly.

(20) Disconnect both ends of resistors from mounting disks (3, fig. 3-17).

(21) Remove spacer (5) from resistor module.

(22) Remove mounting disk (3) and resistors (4) from assembly.

(23) Remove screw (2) from hex spacer and standoff (2).

(24) Remove mounting disk from hex spacer.

NOTE

To disassemble transformers T2, T3, T4 (fig. 3-16, sheet 1), proceed as follows. Instructions are given for the removal of one transformer. If more than one transformer is to be removed, repeat procedure for each transformer to be removed.

(25) Mark and disconnect wires from transformer,

(26) Remove three screws (14, 37, fig. 3-16, sheet 2) from side of inverter chassis.

(27) Remove transformer from inverter chassis.

(28) Note location and remove resistor from transformer.

NOTE

To disassemble transistors Q17 through Q34 (fig. 3-16, sheet 1), proceed as follows. Instructions are given for the removal of one transistor. If more than one transistor is to be removed, repeat procedure for each transistor that is to be removed.

(29) Mark and disconnect wires attached to the base and emitter.

(30) Note location and disconnect diodes if attached to transistor being removed.

(31) Remove screws (5) from transistor. Note order of removal of nut (9), spade lug (10), washers (8), and insulated washer (6).

(32) Remove transistor from chassis.

(33) Remove transistor insulator (11) from transistor.

CAUTION

When assembly of transistors is to be performed, extreme caution shall be taken when assembling insulating material (11) and mounting hardware. Any assembly other than what is indicated by this procedure and figure 3-16 will cause serious damage to the transistor and associated circuitry.

(34) Disassemble regulator assembly A28 and capacitor assembly A29 as required by removing individual components shown on figure 3-20.

NOTE

Identify all wires and connections to capacitors and transformers, and disassembly sequence of transistor Q16 to aid in reassembly.

3-29. Assembly instructions

a. To assemble the PP-7274B/A Static Power Inverter, follow the disassembly instructions in reverse order. When making solder connections, use only approved solder QQ571, part number Sn63-W-RA-P3. After a connection is made, brush on HYSOL 22H to protect solder joints.

b. When assembly of a pulser transistor or inverter transistor is to be made, special care shall be taken when mounting transistor to chassis. Heat conducting grease (MIL-S-8660, Type G624) must be applied to both sides of transistor insulator before transistor is mounted to chassis. When securing transistors to chassis, special care must be taken to mount hardware and insulating hardware by reversing the order described in the disassembly instructions (para 3-28(3) and 3-28(4)). To ensure that the transistors are mounted properly, connect the positive lead of an ohmmeter to the case (collector) of the transistor and the negative lead to the chassis (ground); the resistance shall read infinite (check before wires are connected). If the resistance reads zero ohms, or a low value, disassemble transistor and reassemble as described in paragraphs 3-28(3) and 3-28(4).

Table 3-9. Output Distortion Test Parameters

* LOAD	INPUT VOLTS VDC	INPUT AMPS MAX	OUTPUT VOLTS VAC	OUTPUT AMPS	OUTPUT FREQUENCY Hz	THERMAL HARMONIC FREQUENCY	POWER FACTOR
A	28	41	115.5	2.18	400±7	5% MAX	- .95
A	26	44.4	115.5	2.18	400±7	5% MAX	+1.0
A	29	39.8	115.5	2.18	400±7	5% MAX	+ 1.0
B	26	33.3	115.5	2.18	400±7	5% MAX	- .95
B	28	30.8	115.5	2.18	400±7	5% MAX	- .95
B	29	29.9	115.5	2.18	400±7	5% MAX	- .95
C	26	42.2	115.5	2.18	400±7	5% MAX	+ .75
C	28	38.9	115.5	2.18	400±7	5% MAX	+ .75
C	29	37.8	115.5	2.18	400±7	5% MAX	+ .75

* Load A–Resistive load 52.9 ohms ±1%.
Load B–Inductive load 28.5 mh ±3% in parallel withs 70.6 ohms ± 1% resistor.
Load C–Capacitive load 2.3 uf ± 3% in parallel with a 55.7 ohms ±1% resistor.

Section V. FINAL TESTS

3-30. General

a. The following test procedures shall be used to be sure that the inverter is ready for operational use. To qualify as operational, all performance standards shall be met. Failure of any one test will fail the unit and not qualify it for field use.

b. Special attention to test equipment control settings shall be made. Adherence to testing sequence is mandatory. Test equipment control settings and inverter measurements can be used in subsequent tests.

c. If during testing it is determined that an adjustment must be made to bring the unit to acceptable standards, all previous tests shall be repeated to be sure that no other test measurement has changed.

3-31. Physical Test and Inspection of the Inverter

a. Test Equipment and Materials Tool Kit TK-100.
b. Test Connections and Conditions. None required.
c. Initial Test Equipment Settings. None required.
d. Procedure. Tests shall be performed in the order presented in the chart below:

step No.	Control settings: Test Equipment	Control settings: Equipment Under Test	Test procedure	Performance standard
	N/A	N/A	*a.* Inspect all assemblies for loose or missing screws.	*a.* Screws shall be tight none missing.
			b. Inspect all surfaces for dents, scratches and gouges.	*b.* There shall be no dents, scratches or gouges.
			c. Inspect all painted surfaces for chips or excessive wear.	*c.* There shall be no chips or sign of excessive wear.
			d. Inspect all electronic connections and electronic components for fungus proofing.	*d.* All connections shall be coated with HYSOL 22H.

LEGEND

REF. DES.	ITEM NO.	REF. DES.	ITEM No.
C101	1	Q115	19
C102	2	R101	21
C103	3	R102	22
C104	4	R103	21
C105	2	R1M	23
C106	5	R105	24
C107	6	R106	24
C108	7	R107	25
C109	8	R108	26
C110	9	R109	27
C111	10	RIIO	26
C112	11	RIII	28
C113	1	RII2	29
C114	11	RII3	30
CR101	12	RII4	24
CR102	13	RII5	31
CR103	13	RII6	32
CR104	14	RII7	33
CR105	15	RII8	32
CR106	15	RII9	29
CR107	15	RI20	34
CR108	15	RI2I	35
CR109	15	RI22	36
CRIIO	12	RI23	37
CRIII	12	RI24	38
CRII2	15	RI25	3?
CRII3	15	RI26	40
CRII4	12	RI27	41
LI0I	16	RI28	28
Q10I	17	RI29	42
Q102	18	RI30	43
Q103	19	RI3I	29
Q104	19	RI32	29
Q105	20	RI33	44
Q106	19	RI34	29
Q107	19	RI35	23
Q108	19	RI36	45
Q109	17	RI37	46
QIIO	18	RI38	47
QIII	18	RI39	48
QII2	19	RI40	48
QII3	19	RI4I	48
QII4	19	RI42	49

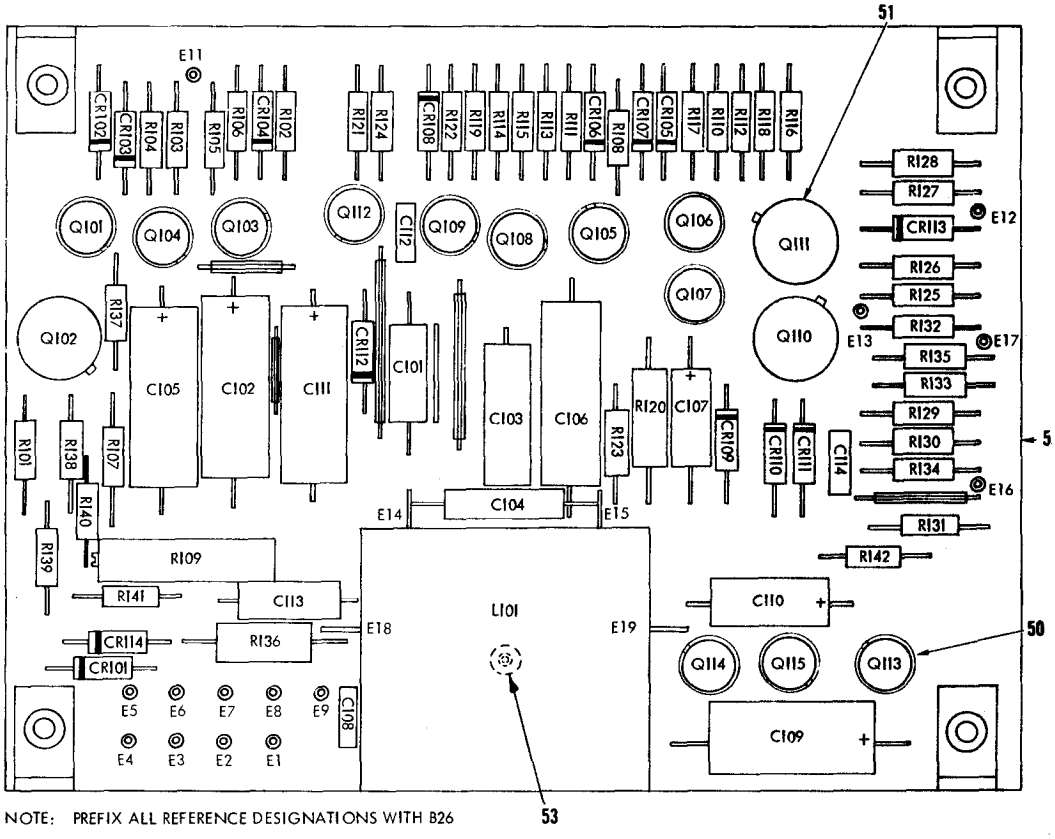


Figure 3-18. B26 Printed Circuit Board.

3-32. Final Test for Static Inverter

a. Test Equipment and Materials. Test equipment shall be as shown in test fixture diagram (fig. FO-6) and test equipment list (table 3-3).

b. Test Connections and Conditions. Connect test equipment as indicated in figure FO-6.

c. Initial Test Equipment Settings.

(1) Activate all test equipment and let stabilize for one-half hour.

(2) Turn power supply output voltage to zero before connecting supply to inverter.

d. Procedure. Tests shall be performed in the order presented in table 3-10.

LEGEND

REF. DES.	ITEM NO.	REF. DES.	ITEM NO.	REF. DES.	ITEM NO.
C1	1	CR110	9	R15	28
C2	2	L1	11	R16	29
C3	3	L101	11	R17	30
C4	4	Q1	12	R18	31
C5	5	Q2	13	R19	32
C6	6	Q3	12	R20	18
C7	7	Q4	13.1	R21	33
C8	2	Q5	14	R22	31
C9	8	Q6	12	R23	23
C101	1	Q7	12	R24	19
C102	2	Q8	12	R25	34
C103	3	Q9	14	R101	15
C104	4	Q10	12	R102	16
C105	5	Q101	12	R103	17
C106	6	Q102	13	R104	18
C107	7	Q103	12	R105	19
C108	2	Q104	13.1	R106	18
C109	8	Q105	14	R107	20
CR1	9	Q106	12	R108	21
CR2	10	Q107	12	R109	22
CR3	10	Q108	12	R110	23
CR4	10	Q109	14	R111	35
CR5	10	Q110	12	R112	25
CR6	10	R1	15	R113	26
CR7	10	R2	16	R114	27
CR8	10	R3	17	R115	28
CR9	9	R4	18	R116	29
CR10	9	R5	19	R117	30
CR101	9	R6	18	R118	31
CR102	10	R7	20	R119	32
CR103	10	R8	21	R120	18
CR104	10	R9	22	R121	33
CR105	10	R10	23	R122	31
CR106	10	R11	24	R123	23
CR107	10	R12	25	R124	19
CR108	10	R13	26	R125	34
CR109	9	R14	27		

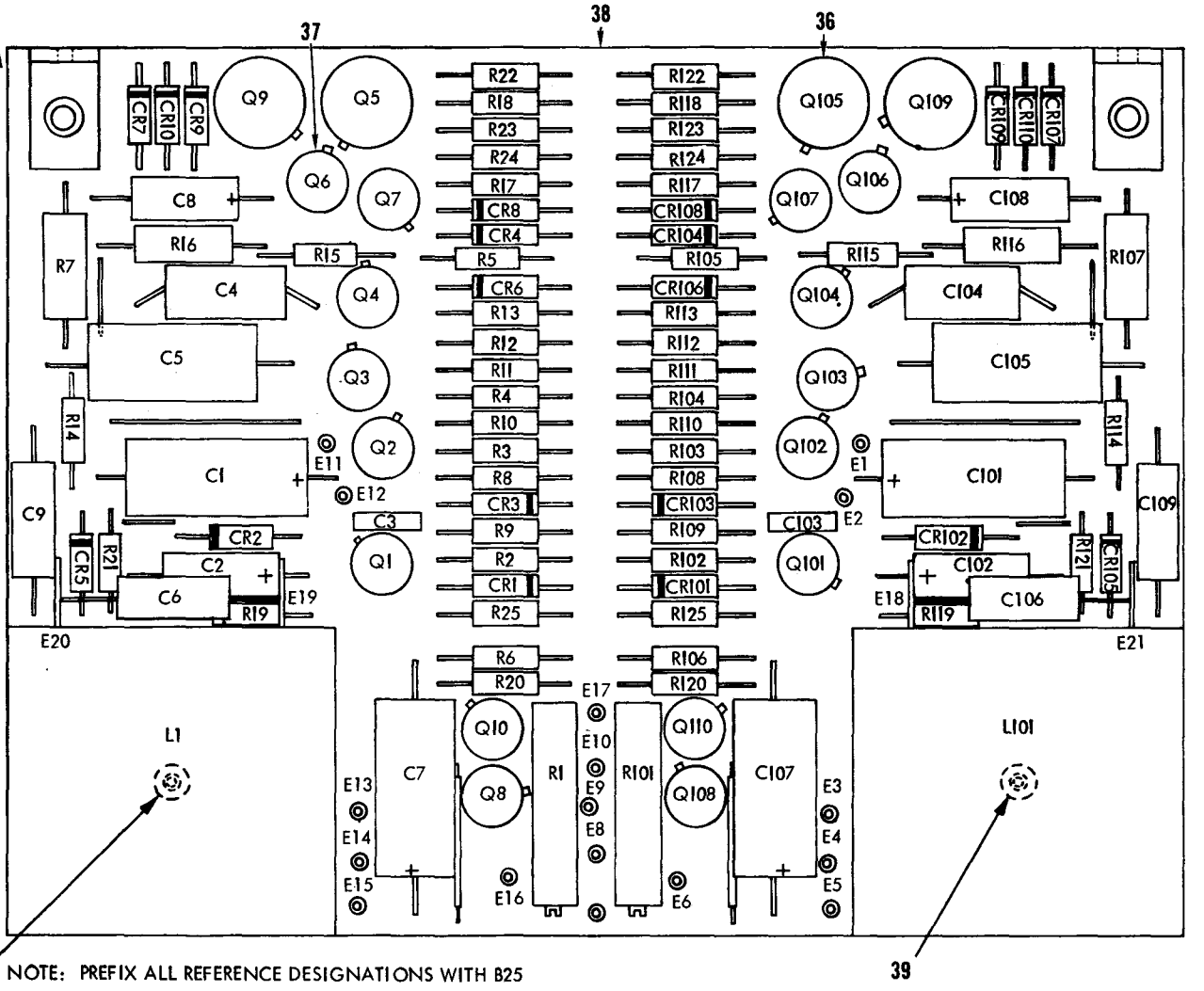
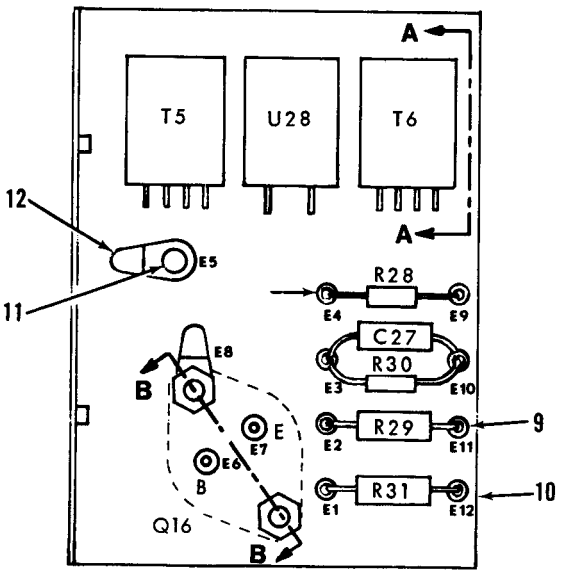
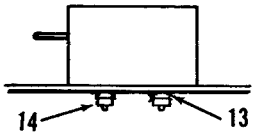


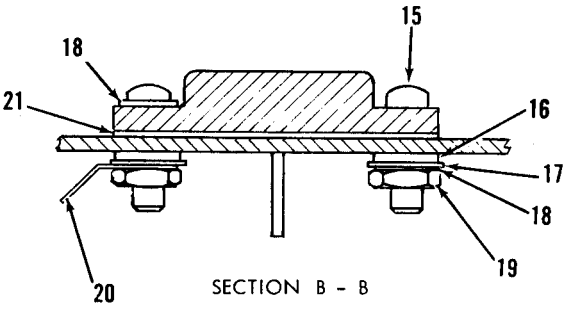
Figure 3-19. B25 Printed Circuit Board.



REF DES	ITEM NO.
C27	1
Q16	2
R28	3
R29	4
R30	5
R31	6
T5	7
T6	7
U28	8



SECTION A - A



SECTION B - B

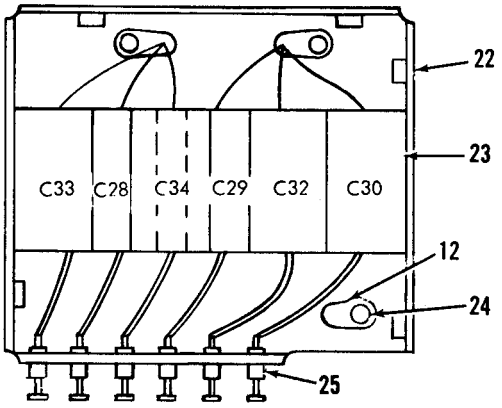


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Figure 3-20. Regulator Assembly A28 and Capacitor Assembly A29.

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	Refer to column 2 table 3-10.	Refer to column 10 table 3-10.	*a.* Set output load conditions.	*a.* Switches shall be as described in table 3-10, column 2.
			b. Adjust input voltage.	*b.* Voltage shall be as described in table 3-10, column 3.
			c. Adjust power setting.	*c.* Power setting shall be as shown in table 3- 10, column 5.
			d. Measure and record: (1) Input current (2) Output current (3) Voltage (4) Frequency (5) Distortion	*d.* Refer to table 3-10, columns 4, 5,6,7, 8,9 for limits.
			e. Measure and record (1) Input current (2) Output voltage (3) Output current with input voltage set at 26 and 29 vdc.	*e.* Refer to table 3-10, columns 4, 6, 7, 8 for limits.
2	N/A	N/A	Repeat steps 1 *a* through 1 *e* until all sections of table 3-10 have been completed.	Tests will be performed in the order presented in table 3-10.

Table 3-10. Distortion Test Specifications

1	2						3	4	5	6	7	8	9	10
TEST NO.	TEST FIXTURE SWITCH POS. S1	S2	S3	S4	S5	S6	INPUT VOLTAGE VDC(±.01)	INPUT CURRENT (AMPS)	POWER SETTING (WATTS)	OUTPUT CURRENT	OUTPUT VOLTAGE VAC(-2.5)	OUTPUT FREQ. (HERTZ)	OUTPUT DIST. (MAX)	TEST
1	NL	Y	ØA	+1	OFF	OFF	+18	12	N/A		100	400 ±7	20%	NO LOAD Y MODE
2	NL	Y	ØA	+1	OFF	OFF	28	9.3	N/A	2.18	115.0	400 ±7	5%	
3							26 & 29	10 9	N/A	2.18	115.0	N/A	5%	
4	NL	Y	ØB	+1	OFF	OFF	28	9.3	N/A	2.18	115.0	400 ±7	5%	
5							26 & 29	10 9	N/A	2.18	115.0	N/A	5%	
6	NL	Y	ØC	+1	OFF	OFF	28	9.3	N/A	2.18	115.0	400 ±7	5%	
7							26 & 29	10 9	N/A	2.18	115.0	N/A	5%	
8	FL	Y	ØA	+1	ØA	OFF	28	41	250 ±.5	2.18	115.0	400 ±7	5%	FULL LOAD Y MODE
9							26 & 29	44.4 39.8	250 ±.5	2.18	115.0	N/A	5%	
10	FL	Y	ØB	+1	ØB	OFF	28	41	250 ±.5	2.18	115.0	400 ±7	5%	
11							26 & 29	44.4 39.8	250 ±.5	2.18	115.0	N/A	5%	
12	FL	Y	ØC	+1	ØC	OFF	28	41	250 ±.5	2.18	115.0	400 ±7	5%	
13							26 & 29	44.4 39.8	250 ±.5	2.18	115.0	N/A	5%	
14	FL	Y	ØA	-.95	ØA	OFF	28	30.8	237 ±.5	2.18	115.0	400 ±7	5%	
15							26 & 29	33.3 29.9	237 ±.5	2.18	115.0	N/A	5%	
16	FL	Y	ØB	-.95	ØB	OFF	28	30.8	237 ±.5	2.18	115.0	400 ±7	5%	
17							26 & 29	33.3 29.9	237 ±.5	2.18	115.0	N/A	5%	

Table 3-10. Distortion Test Specifications - Continued

1	2						3	4	5	6	7	8	9	10
TEST NO.	TEST FIXTURE SWITCH POS. S1	S2	S3	S4	S5	S6	INPUT VOLTAGE VDC(±.01)	INPUT CURRENT (AMPS)	POWER SETTING (WATTS)	OUTPUT CURRENT	OUTPUT VOLTAGE VAC(-2.5)	OUTPUT FREQ. (HERTZ)	OUTPUT DIST. (MAX)	TEST
18	FL	Y	ØC	-.95	ØC	OFF	28	30.8	237 ±.5	2.18	115.0	400 ±7	5%	
19							26 & 29	33.3 29.9	237 ±.5	2.18	115.0	N/A	5%	
20	FL	Y	ØA	+.75	ØA	OFF	28	38.0	187 ±.5	2.18	115.0	400 ±7	5%	
21							26 & 29	42.2 37.8	187 ±.5	2.18	115.0	N/A	5%	
22	FL	Y	ØB	+.75	ØB	OFF	28	38.9	187 ±.5	2.18	115.0	400 ±7	5%	
23							26 & 29	42.2 37.8	187 ±.5	2.18	115.0	N/A	5%	
24	FL	Y	ØC	+.75	ØC	OFF	28	38.9	187 ±.5	2.18	115.0	400 ±7	5%	
25							26 & 29	42.2 37.8	187 ±.5	2.18	115.0	N/A	5%	
26	FL		ØA	+1	ØA	OFF	28	41	250 ±.5	2.18	115.0	400 ±7	5%	FULL LOAD DELTA MODE
27							26 & 29	44.4 39.8	250 ±.5	2.18	115.0	N/A	5%	
28	FL		ØB	+1	ØB	OFF	28	41	250 ±.5	2.18	115.0	400 ±7	5%	
29							26 & 29	44.4 39.8	250 ±.5	2.18	115.0	N/A	5%	
30	FL		ØC	+1	ØC	OFF	28	41	250 ±.5	2.18	115.0	400 ±7	5%	
31							26 & 29	44.4 39.8	250 ±.5	2.18	115.0	N/A	5%	

3-33. Final Check of Short Circuit Shutdown Circuitry

a. Connect inverter to test fixture as shown in figure FO-6.

b. Set test fixture switches as follows: S-l–No load; S-2–Wye; S-3–Phase A; S-4–+1.0; S-5–Phase A.

c. Preset load variacs for minimum load.

d. Apply +28±.01 vdc to inverter input.

e. Set S- 1 to load.

f. Adjust phases A, B and C for a reading of 250 on the power meter. Switch settings for each phase are as follows:

(1) Phase A–S-5 to phase A adjust variac TA.

(2) Phase B–S-5 to phase B adjust variac TB.

(3) Phase C–S-5 to phase C adjust variac TC.

g. Measure and record voltage, distortion and frequency for each phase.

h. Measure and record input current.

i. Using a stopwatch, measure time required for input current to fold back (reduce to approximately one-half the value recorded in *g* above) when S-6 is pressed.

NOTE

S-6 is a momentary contact switch. It will be necessary to hold the actuator down until the input has folded back.

NOTE

Input current should be approximately 35 to 40 amperes.

j. Press S-6 and measure time. Current should fold back in less than 20 seconds, but more than 5 seconds.

k. Release S-6 after current has been reduced.

l. Record elapsed time.

NOTE

If current was excessive, troubleshoot inverter as described in paragraph 3-8. If unit failed time limits, adjust inverter as described in paragraph 3-26.

m. To measure recovery time of inverter, proceed as follows:

(1) Press S-6 and hold until unit folds back.

(2) Measure time required for unit to recover to value recorded in g above when S-6 is released.

NOTE

Time shall be less than 0.5 second.

(3) Record recovery time.

(4) Measure and record output voltage, frequency and distortion. Readings should be less than 1% or identical to the readings recorded in *h* above.

(5) Set S-1 to no Load.

(6) Turn input power off.

3-34. Wire Lists

Table 3-11. Wire List

Subparagraphs *a* through *i* below list the wire runs for each major unit of the PP-7274B/A.

a. Power Transformer T1-A. T1-B. T1-C)

Wire No.	Termination		Wire color
	From	To	
1	T1-A-1	A27A1	Gry
2	2	A27A2	Wht/Gry
3	5	A2Q26-C	Gry
4	5	A2Q28-C	Gry
5	6	B25E2	Red
6	6	A1L202	Brn
7	6	A1L4-2	Brn
8	7	A2Q19-C	Red
9	7	A2Q17-C	Red
10	T1-B-1	A27B2	Blk
11	2	A2T7-3	Wht/Blk
12	5	A2Q29-C	Wht
13	5	A2Q31-C	Wht
14	6	A1L5-2	Vio
15	6	B26E7	Vio
16	6	A1L7-2	Vio
17	7	A2Q22-C	Yel
18	7	A2Q20-C	Yel
19	T1-C-1	A27A2	Blu
20	2	A27A1	Wht/Blu
21	5	A2Q34-C	Blu
22	5	A2Q32-C	Blu/Wht
23	6	A1L7-2	Grn
24	6	B25E12	Wht/Red
25	6	A1L9-2	Grn
26	7	A2Q23-C	Red
27	7	A2Q25-C	Red

Table 3-11. Wire List

b. Transformers T2, T3, T4, T5, T6, T7

Wire No.	Termination		Wire color
	From	To	
1	A2T2-1	B25E5	Grn
2	2	A1T3-2	Wht/Vio
3	3	B25E4	Yel
4	4	A23-1B-3	Brn
5	5	A2R25	Self Lead
6	5	B25E3	Orn
7	6	A23-1B-6	Orn
8	7	A2Q17-E	Orn
9	7	A2Q19-E	Orn
10	8	GND	
11	9	A2Q26-E	Brn
12	9	A2Q28-E	Brn
13	A2T3-1	B26-1	Brn
14	2	A2T4-2	Wht/Vio
15	3	B26-9	Wht
16	4	A23-2B-3	Brn
17	5	A2R26	Self Lead
18	5	B26-8	Gry
19	6	A23-2B-6	Orn
20	A2T3-7	A2Q20-E	Brn
21	7	A2Q22-E	Brn
22	8	GND	
23	9	A2Q29-E	Brn
24	9	A2Q31-E	Brn
25	A2T4-1	B25-14	Wht/Yel
26	2	A28E7	Wht/Vio
27	3	B25-15	Wht/Grn
28	4	A23-3B-3	Brn
29	5	A2R27	Self Lead
30	5	B25-13	Wht/Orn
31	6	A23-3B-6	Orn
32	7	A2Q23-E	Orn
33	7	A2Q25-E	Orn
34	8	GND	
35	9	A2Q32-E	Brn
36	9	A2Q25-E	Brn
37	B28T5-1	A5-11	Wht/Brn
38	2	A5-4	Wht/Red
39	B28T5-3	GND	Ins. Buss
40	4	B28U28-4	Ins. Buss
41	B28T6-1	A5-10	Brn
42	2	A5-12	Red
42A	3	T5-3	Ins. Buss
43	4	B28U28-2	Ins. Buss
44	A2T7-1	A2C34	Self Lead
45	1	Fan-2	Grn
46	2	GND	Blk
47	3	T1-B-2	Wht/Blk
48	4	A27B2	Wht

Table 3-11. Wire List

c. Printed Circuit Board Regulator Assembly B28

Wire No.	Termination		Wire color
	From	To	
1	B28T5-1	A5-11	Wht/Blu
2	2	A5-4	Wht/Red
3	3	B28E5	Ins. Buss
4	4	B28U28-4	Ins. Buss
5	B28T6-1	A5-10	Brn
6	2	A5-12	Red
7	3	B28E5	Ins. Buss
8	4	B28U28	Ins. Buss
9	B28E2	B26-E6	Blu
10	B28E1	A5-5	Blu
11	B28E9	B25E20	Brn/Blk
12	B28U28-1	B25E16	Blu
13	2	B28T6-4	Ins. Buss
14	3	B25E6	Wht/Blu
15	4	B28T5-4	Ins. Buss
16	B28E7(Q16E)	A2T2-4	Wht/Vio
17	B28E6(Q16B)	B26E5	Grn
18	B28E8(Q16C)	B26E4	Yel
19	B28E9(Q16C)	A2L1-2	Yel
20	B28E3	B28E11	Ins. Buss
21	B28E9	B28E10	Ins. Buss
22	B28E12	B28E2	Ins. Buss
23	B28E3	B28E5	Blk
24	B28E1	B28E4	Ins. Buss
25	B28E7	B25E17	Wht/Vio

Table 3-11. Wire List

d. Printed Circuit Board Phase A Board B26.

Wire No.	Termination		Wire color
	From	To	
1	B26-1	A2T3-1	Brn
2	2	A1R5	Red
3	3	GND	Blk
4	4	B28Q16-C	Yel
5	4	A1Q12-C	Yel
6	5	B28Q16-B	Grn
7	5	B28E6	Grn
8	6	A28E13	Blu
9	7	T1-B-6	Vio
10	8	A2T3-5	Gry
11	9	A2T3-3	Wht
12	10	NC	
13	11	B25E10	Wht
14	12	B25E7	Vio
15	13	B25E8	Gry
16	14	B26C104	
17	15	B26C104	
18	16	NC	
19	17	NC	
20	18	B25E18	Wht/Gry
21	19	B25E19	Wht/Blk

Table 3-11. Wire List

e. Printed Circuit Board Phase B and C Board B25.

Wire No.	Termination		Wire color
	From	To	
1	B25-1	A1R4	Brn
2	2	T1-A-6	Red
3	3	A2T2-5	Orn
4	4	A2T2-3	Yel
5	5	A2T2-1	Grn
6	6	B28U28-3	Wht/Blu
7	7	B26E12	Vio
8	8	B26E13	Gry
9	9	GND	Blk
10	10	B26E11	Wht
11	11	A1R6	Wht/Brn
12	12	T1-C-6	Wht/Red
13	13	A2T4-5	Wht/Orn
14	14	A2T4-1	Wht/Yel
15	15	A2T4-3	Wht/Grn
16	16	A28U28-1	Blu
17	17	A28E7	Wht/Vio
18	18	B26E18	Wht/Orn
19	19	B26E19	Wht/Blk
20	*20*	B28E9	Brn/Blk

Table 3-11. Wire List

f. Fan and Filter Assembly, Fan B1 I/O Filter A5.

Wire No.	Termination		Wire color
	From	To	
1	B1-1	GND	Blk
2	B1-2	A2T7-1	Grn
3	B1-2	B1C35	Self Lead
4	B1-3	B1C35	Self Lead
1	A5-1	A27A-1	Wht/Blu
2	2	A27C-1	Gry
3	3	A27B-2	Wht/Blk
4	4	B28T5-2	Wht/Gry
5	5	B28R29	Wht/Blk
6	6	GND	
7	7	A27C-2	Gry
8	8	GND	
9	9	A27A-2	Blu
10	10	B28T6-1	Brn
11	11	B28T5-1	Wht/Brn
12	12	B28T6-2	Wht/Blu

Table 3-11. Wire List

g. Inverter Assembly A2.

Wire No.	Termination		Wire color
	From	To	
1	A2Q17-E	A2T2-7	Brn
2	B	A23-1A-1	Brn
3	C	T1-A-7	Red
4	C	A2CR13-C	Self Lead
5	A2Q18-E	A2Q17-E	Brn
6	E	A2Q19-E	Brn
7	E	A2CR10-A	Self Lead
8	B	A23-1A-2	Brn
9	C	A2Q17-C	Yel
10	C	A2Q19-C	Yel
11	C	A2CR13-C	Self Lead
12	A2Q19-E	A2T2-7	Brn
13	B	A23-1A-3	Brn
14	C	T1-A-7	Red
15	C	A29-2	Yel
16	A2Q20-E	A2T3-7	Brn
17	B	A23-2A-1	Brn
18	C	T1-B-7	Yel
19	C	A2CR14-2	Self Lead
20	A2Q21-E	A2Q20-E	Brn
21	A2Q21-E	A2Q22-E	Brn
22	E	A2CR11-A	Self Lead
23	B	A23-2A-2	Brn
24	C	A2Q20-C	Blu
25	C	A2Q22-C	Blu
26	A2Q22-E	A2T3-7	Brn
27	B	A23-2A-3	Brn
28	C	T1-B-7	Yel
29	C	A29-4	Blu
30	A2Q23-E	A2T4-7	Brn
31	B	A23-3A-1	Brn
32	C	T1-C-7	Red
33	A2Q24-E	A2Q23-E	Brn
34	E	A2Q25-E	Brn
35	B	A23-3A-2	Brn
36	C	A2Q23-C	Gry
37	C	A2Q25-C	Gry
38	A2Q25-E	A2T4-7	Brn
39	E	A2CR12-A	Self Lead
40	B	A23-3A-3	Brn
41	A2Q25-C	T1-C-7	Red
42	C	A2CR15-C	Self Lead
43	C	A29-6	Gry
44	A2Q26-E	A2T2-9	Orn
45	B	A23-1A-4	Orn
46	C	T1-A-5	Gry
47	C	A2C10-C	Self Lead
48	A2Q27-E	A2Q26-E	Orn
49	E	A2Q28-E	Orn
50	E	A2CR13-A	Self Lead
51	B	A23-1A-5	Orn
52	C	A2Q26-C	Grn
53	C	A2Q28-C	Grn
54	A2Q28-E	A2T2-9	Orn
55	B	A23-1A-6	Orn
56	C	T1-A-5	Gry
57	C	A29-3	Grn
58	A2Q29-E	A2T3-9	Orn
59	E	A2CR14-A	Self Lead
60	B	A23-2A-4	Orn
61	A2Q29-C	T1-B-5	Wht

Table 3-11. Wire List

g. Inverter Assembly A2-Continued

Wire No.	Termination		Wire color
	From	To	
62	C	A2CR11-C	Self Lead
63	A2Q30-E	A2Q29-E	Orn
64	E	A2Q31-E	Orn
65	B	A23-2A-5	Orn
66	C	A2Q29-C	Vio
67	C	A2Q31-C	Vio
68	A2Q31-E	A2T3-9	Orn
69	B	A23-2A-6	Orn
70	C	T1-B-5	Wht
71	C	A29-5	Vio
72	A2Q32-E	A2T4-9	Orn
73	B	A23-3A-4	Orn
74	C	T1-C-5	Blu
75	A2Q33-E	A2Q32-E	Orn
76	E	A2Q34-E	Orn
77	B	A23-3A-5	Orn
78	C	A2Q32-C	Wht
79	C	A2Q34-C	Wht
80	C	A2CR12-C	Self Lead
81	A2Q34-E	A2T4-9	Orn
82	E	A2CR15-A	Self Lead
83	B	A23-3A-6	Orn
84	C	T1-C-5	Blu
85	C	A29-1	Wht

Table 3-11. Wire List

h. Pulser Assembly A1

Wire No.	Termination		Wire color
	From	To	
1	A1Q1-E	A1Q2-C	Red
2	B	A1Q13-E	Blu
3	C	A1Q2-B	Orn
4	C	A1Q3-B	Orn
5	C	A1Q4-B	Orn
6	A1Q2-E	A1CR1-C	Yel
7	E	A1L2-1	Yel
8	B	A1Q1-C	Orn
9	C	A1Q3-C	Red
10	C	+28 vdc	Red
11	A1Q3-E	A1CR2-C	Yel
12	E	A1L3-1	Yel
13	B	A1Q1-C	Orn
14	C	A1Q4-C	Red
15	C	+28 vdc	Red
16	A1Q4-E	A1CR3-C	Yel
17	E	A1L4-1	Yel
18	B	A1Q1-C	Orn
19	C	A1Q6-C	Red
20	C	+28 vdc	Red
21	A1Q5-E	A1Q6-C	Red
22	B	A1Q14-E	Blu
23	C	A1Q6-B	Orn
24	C	A1Q7-B	Orn
25	C	A1Q8-B	Orn
26	A1Q6-E	A1CR4-C	Yel
27	E	A1L5-1	Yel
28	B	A1Q5-C	Orn
29	C	A1Q7-C	Red
30	C	+28 vdc	Red

Table 3-11. Wire List

h. Pulser Assembly A1–Continued

Wire No.	Termination		Wire color
	From	To	
31	A1Q7-E	A1CR5-C	Yel
32	E	A1L6-1	Yel
33	B	A1Q5-C	Orn
34	C	A1Q8-C	Red
35	C	+28 vdc	Red
36	A1Q8-E	A1CR6-C	Yel
37	E	A1L7-1	Yel
38	B	A1Q5-C	Orn
39	C	A1Q10-C	Red
40	C	+28 vdc	Red
41	A1Q9-E	A1Q10-C	Red
42	B	A1Q15-E	Blu
43	C	A1Q10-B	Orn
44	C	A1Q11-B	Orn
45	C	A1Q12-B	Red
46	A1Q10-E	A1CR7-C	Yel
47	E	A1L8-1	Yel
48	B	A1Q9-C	Orn
49	C	A1Q11-C	Red
50	C	+28 vdc	Red
51	A1Q11-E	A1L9-1	Yel
52	E	A1CR8-C	Yel
53	B	A1Q9-C	Orn
54	C	A1Q12-C	Red
55	C	+28 vdc	Red
56	A1Q12-E	A1CR9-C	Yel
57	E	A1L10-1	Yel
58	B	A1Q9-C	Red
59	C	+28 vdc	Red
60	A1Q13-E	A1Q1-B	Blu
61	B		
62	C	A1CR1-C	Yel
63	A1Q14-E	A1Q5-B	Blu
64	B		
65	C	A1CR4-C	Yel
66	A1Q15-E	A1Q9-B	Blu
67	B		
68	C	A1CR7-C	Brn
69	A1L2-2	A1L3-2	Brn
70	2	T1-A-6	Brn
71	A1L3-2	A1L4-2	Brn
72	2	A1E4	Vio
73	A1L4-2	T1-A-6	Brn
74	A1L5-2	A1L6-2	Vio
75	2	T1-B-6	Vio
76	A1L6-2	A1L7-2	Vio
77	2	A1E5	Grn
78	A1L7-2	T1-B-6	Vio
79	2	A1L6-2	Vio
80	A1L8-2	A1L9-2	Grn
81	2	T1-B-6	Grn
82	A1L9-2	A1L10-2	Grn
83	2	A1E6	Grn
84	A1L10-2	T1-C-6	Grn
85	A1CR1-A-A1CR9-A	GND	Blk
86	A1C1-A1C17	GND	Blk
87	A1C18-A1C26	GND	Blk

Table 3-11. Wire List

i. Resistor Assembly A23

Wire No.	Termination		Wire color
	From	To	
1	A23-1A-1	A2Q17-B	Brn
2	A23-1A-2	A2Q18-B	Brn
3	A23-1A-3	A2Q19-B	Brn
4	A23-1A-4	A2Q26-B	Orn
5	A23-1A-5	A2Q27-B	Orn
6	A23-1A-6	A2Q28-B	Orn
7	A23-1B-1	A23-1B-2	Ins. Bus
8	A23-1B-2	A23-1B-2	Ins. Bus
9	A23-1B-3	A2T2-4	Brn
10	A23-1B-4	A2T2-6	Ins. Bus
11	A23-1B-4	A23-13-5	Ins. Bus
12	A23-1B-5	A2T2-6	Ins. Bus
13	A23-1B-5	A23-1B-6	Ins. Bus
14	A23-1B-6	A2T2-6	Orn
15	A23-2A-1	A2Q20-B	Brn
16	A23-2A-2	A2Qq1-B	Brn
17	A23-2A-3	A2Q22-B	Brn
18	A23-2A-4	A2Q29-B	Orn
19	A23-2A-5	A2Q30-B	Orn
20	A23-2A-6	A2Q31-B	Orn
21	A23-2B-1	A23-2B-2	Ins. Bus
22	A23-2B-2	A23-2B-3	Ins. Bus
23	A23-2B-3	A2T3-4	Brn
24	A23-2B-4	A23-2B-5	Ins. Bus
25	A23-2B-5	A23-2B-6	Ins. Bus
26	A23-2B-6	A2T3-6	Orn
27	A23-3A-1	A2Q23-B	Brn
28	A23-3A-2	A2Q24-B	Brn
29	A23-3A-3	A2Q25-B	Brn
30	A23-3A-4	A2Q32-B	Orn
31	A23-3A-5	A2Q33-B	Orn
32	A23-3A-6	A2Q34-B	Orn
33	A23-3B-1	A23-3B-2	Ins. Bus
34	A23-3B-2	A23-3B-3	Ins. Bus
35	A23-3B-3	A2T4-4	Brn
36	A23-3B-4	A23-3B-5	Ins. Bus
37	A23-3B-5	A23-3B-6	Ins. Bus
38	A23-3B-6	A2T4-6	Orn

APPENDIX A

REFERENCES

Following is a list of references applicable to direct and general support maintenance personnel of Static Power Inverter PP-7274B/A.

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins, Lubrication Orders
DA Pam 310-7	U.S. Army Equipment Index of Modification Work Orders
SB 11-244	Stockage of Signal Items for Use as a Maintenance Float (Exchange)
SB 38-100	Preservation, Packaging and Packing Materials, Supplies, and Equipment used by the Army
TM 11-6625-255-14	Operator's, Organizational, Direct Support and General Support Maintenance Manual: Spectrum Analyzer TS-723A/U, TS-723B/U, TS-723C/U, and TS-723D/U (NSN 6625-00-668-7418)
TM 11-6625-320-12	Operator's and Organizational Maintenance Manual: Voltmeter, Meter ME-30A/U and Voltmeters, Electronic ME-30B/U, ME-30C/U, and ME-30E/U
TM 1l-6625-444-14-1	Operator's, Organizational, Direct Support and General Support Maintenance Manual including Repair Parts and Special Tools Lists: Voltmeter, Digital AN/GSM-64B (NSN 6625-00-022-7894) including Plug-In, Electronic Test Equipment PL-1370/GSM-64B (NSN 6625-00-137-8366)
TM 11-6625-654-14	Operator's, Organizational, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair and Special Tools List) for Multimeter AN/USM-223
TM 11-6625 -700-14-1	Operator, Organizational, Direct Support and General Support Maintenance Manual Including Repair Parts and Special Tools List (Including Depot Repair Parts and Special Tools): Digital Readout Electronic Counter AN/USM-207A (NSN 6625-00-044-3228)
TM 11-6625-2658-14	Operator's, Organizational, Direct Support and General Support Maintenance Manual for Oscilloscope AN/USM-281C (NSN 6625-00-106-9622).
TM 38-750	Army Equipment Record Procedures

ALPHABETICAL INDEX

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL MANUALS

SOMETHING WRONG WITH THIS MANUAL?

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM, TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL!

FROM: (YOUR UNIT'S COMPLETE ADDRESS)
Commander
Stateside Army Depot
ATTN: AMSTA-US
Stateside, N.J. 07703

DATE 10 July 1975

PUBLICATION NUMBER	DATE	TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/[illegible]C-76

BE EXACT...PIN-POINT WHERE IT IS

PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of [illegible] knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

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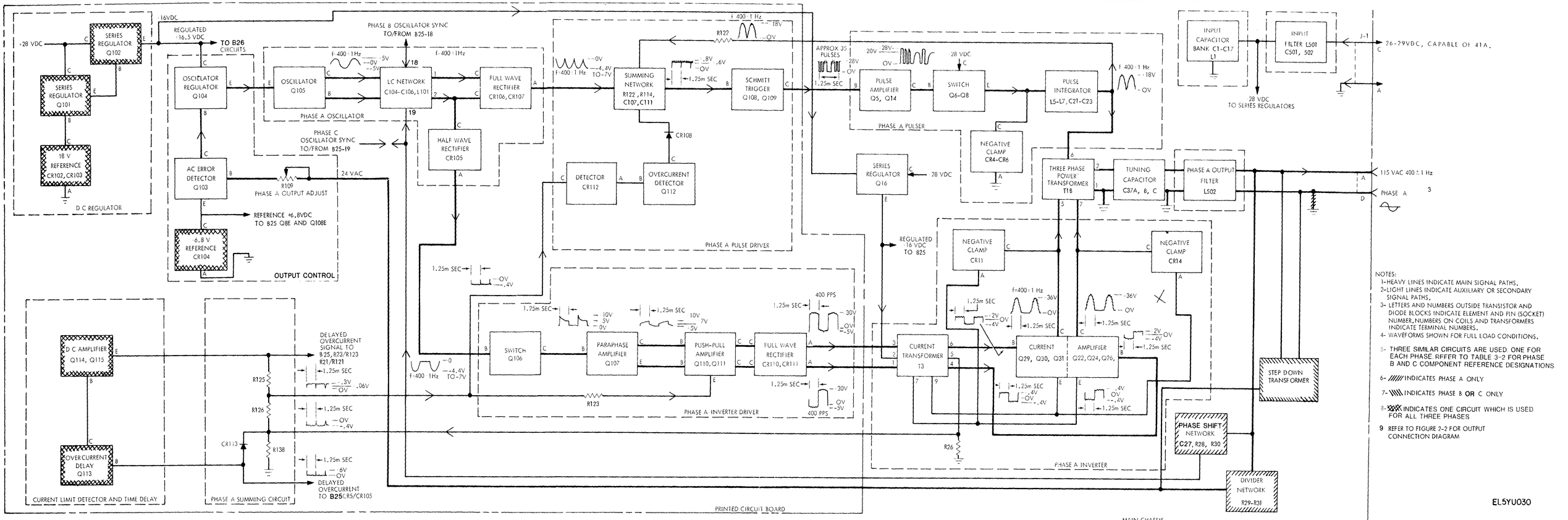


Figure FO-1. Detailed Block Diagram.

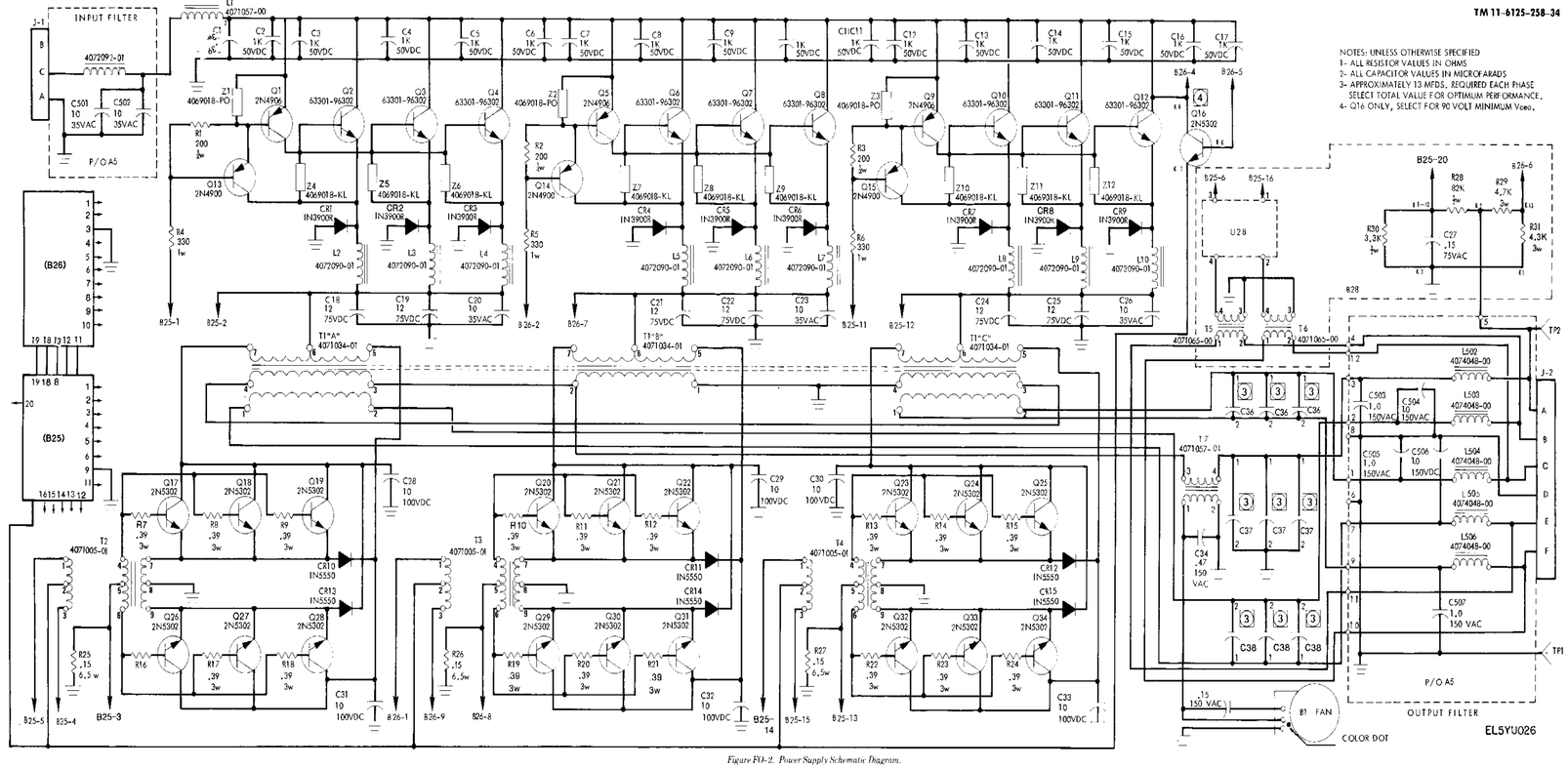


Figure FO-2. Power Supply Schematic Diagram.

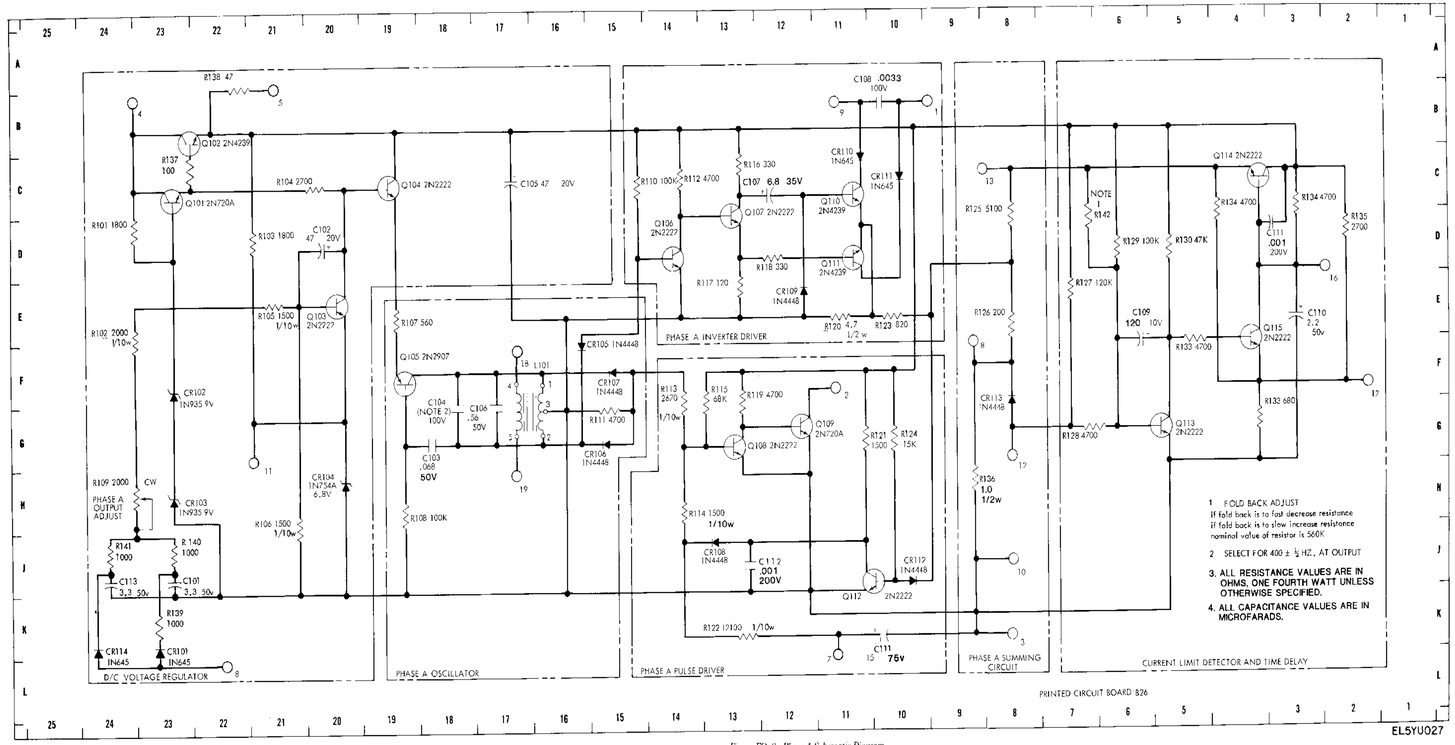


Figure FO-3. Phase A Schematic Diagram.

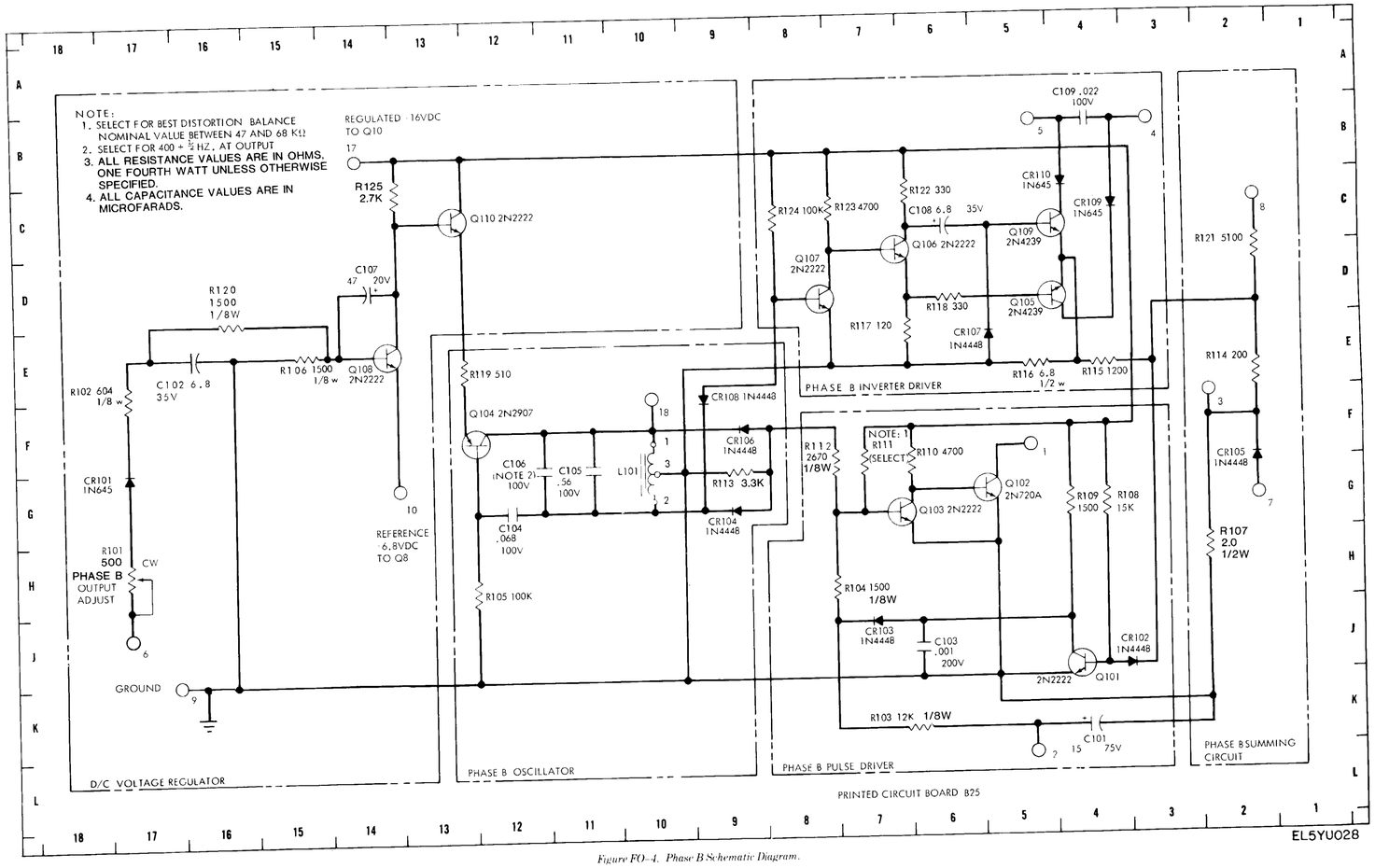


Figure FO-4. Phase B Schematic Diagram.

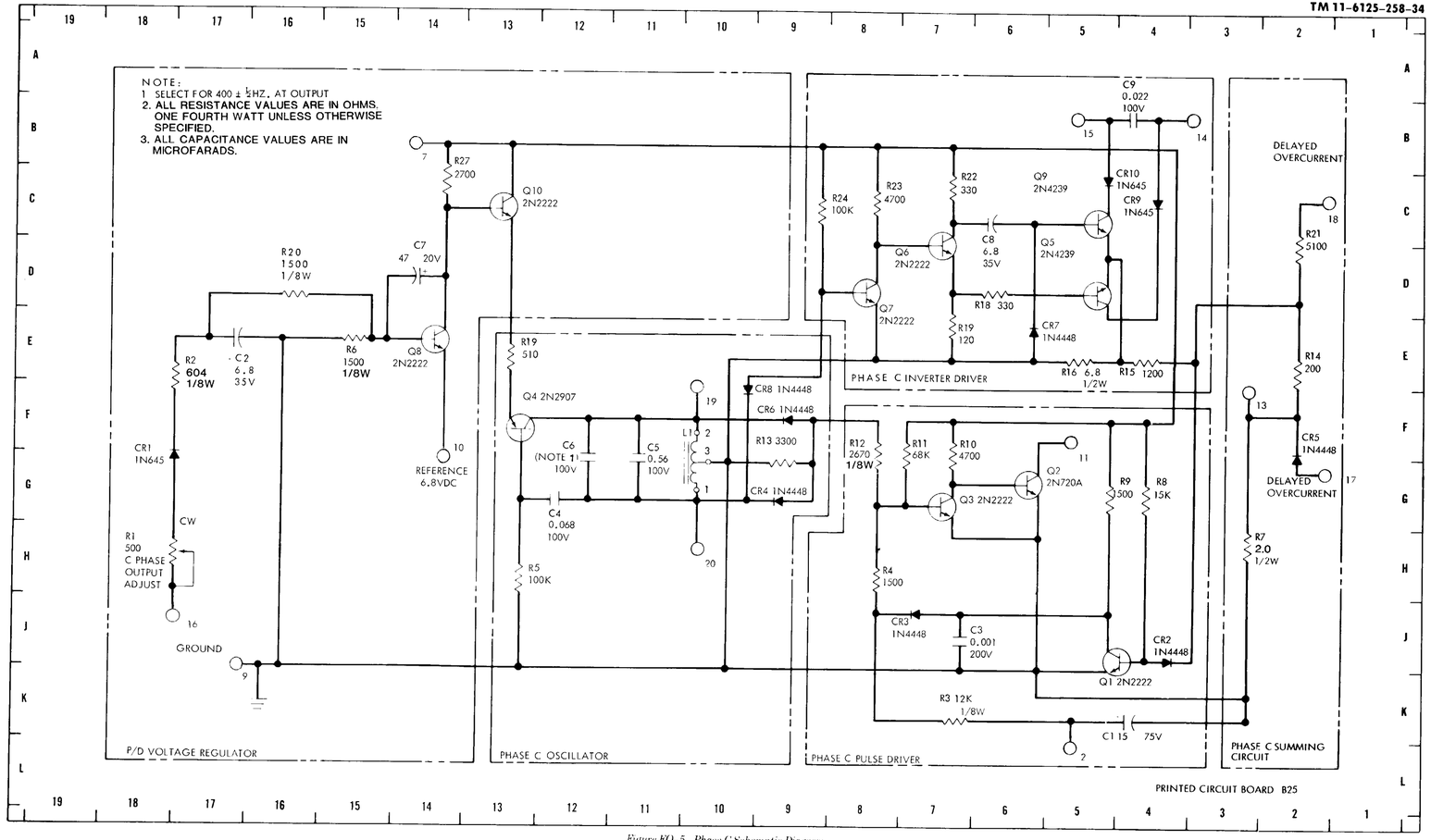
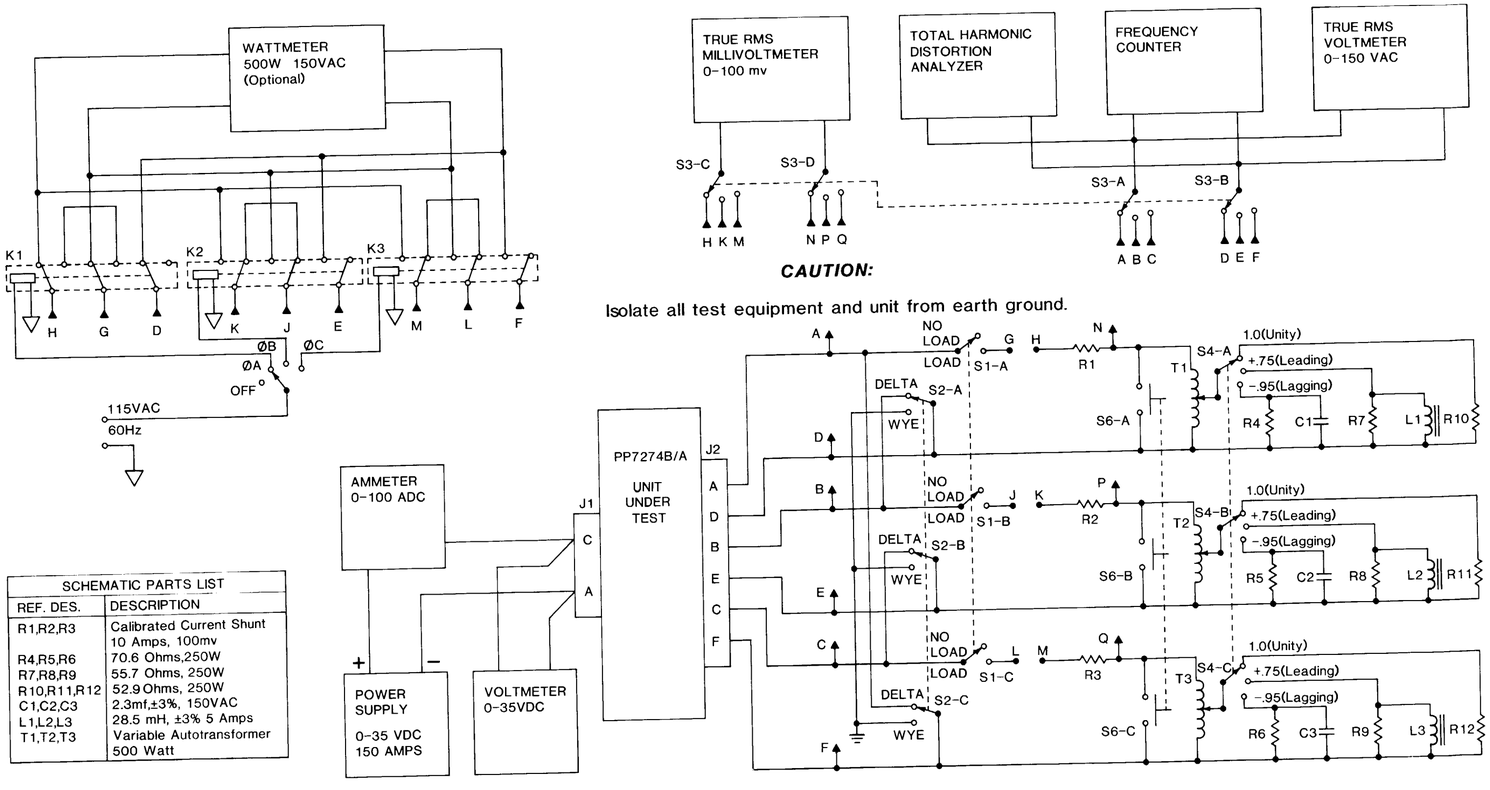


Figure FO-5. Phase C Schematic Diagram.

EL5YU029



SCHEMATIC PARTS LIST	
REF. DES.	DESCRIPTION
R1,R2,R3	Calibrated Current Shunt 10 Amps, 100mv
R4,R5,R6	70.6 Ohms,250W
R7,R8,R9	55.7 Ohms, 250W
R10,R11,R12	52.9 Ohms, 250W
C1,C2,C3	2.3mf,±3%, 150VAC
L1,L2,L3	28.5 mH, ±3% 5 Amps
T1,T2,T3	Variable Autotransformer 500 Watt

CAUTION:

Isolate all test equipment and unit from earth ground.

WARNING: Unit is electrically "HOT" in the DELTA MODE. Touching the unit and ground may cause serious injury or death.

EL5YU03I

NOTE: If wattmeter is not used, jumper G to H, J to K, and L to M.

Figure FO-6. Test Fixture Schematic Diagram.

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General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
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